Thermally Assisted MRAM
How does it work ?

Cristian PAPUSOI, Bernard DIENY
SPINTEC, Grenoble, France

Acknowledgments: O.Redon, A.Astier, (LETI), J.P.Nozières (CROCUS Tech.), S.Cardoso, P.Freitas (INESC-MN Portugal)

Introduction

EDUCATION

1993 – 1998	**Ph. D.**, Faculty of Physics, "Al.I.Cuza" University, Iasi, Romania
1987 – 1992	**Diploma in Physics**, Faculty of Physics, "Al.I.Cuza" University, Iasi, Romania

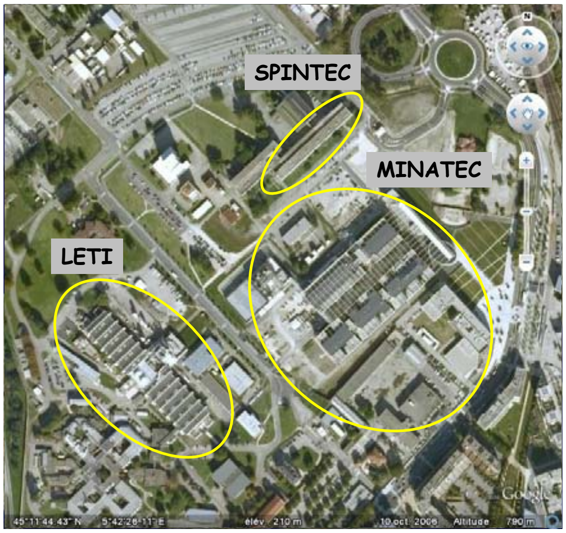
ACADEMIC AND PROFESSIONAL EXPERIENCE

2006 – 2007	**Postdoctoral Research Fellow, Grenoble, France** Investigation of RAM devices with thermal assisted switching
2004 – 2006	**Postdoctoral Research Fellow, Center for Materials for Information Technology (MINT) Center, University of Alabama, Tuscaloosa, USA** Fabrication and characterization of CPP (Current Perpendicular to the Plane) spin valves
2003 – 2004	**Postdoctoral Research Fellow, RWTH University,2 Physikalisches Institut A, Aachen, Germany** Role of non-magnetic defects inserted in metallic antiferromagnets on exchange bias
2000 – 2003	**Postdoctoral Research Fellow, Information Storage Materials Laboratory, Toyota Technological Institute, Nagoya, Japan** Thermal stability and recording performance of hard-disk media
1992 – 2000	**Lecturer**, Department of Electricity and Physical Electronics, Faculty of Physics, "Alexandru Ioan Cuza" University, 11 Blvd. Carol I, 700 506 Iasi, Romania

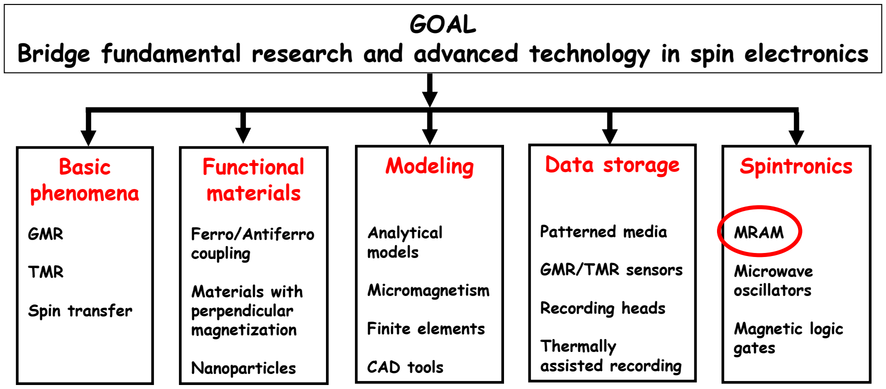
AWARDS

2006	**Outstanding REU student/postdoc mentor**, University of Alabama (11/8/2006)

SPINTEC - location



Main topics of research at SPINTEC



GOAL
Bridge fundamental research and advanced technology in spin electronics

Basic phenomena
- GMR
- TMR
- Spin transfer

Functional materials
- Ferro/Antiferro coupling
- Materials with perpendicular magnetization
- Nanoparticles

Modeling
- Analytical models
- Micromagnetism
- Finite elements
- CAD tools

Data storage
- Patterned media
- GMR/TMR sensors
- Recording heads
- Thermally assisted recording

Spintronics
- MRAM
- Microwave oscillators
- Magnetic logic gates

Created January 2002 as joint CEA/CNRS laboratory affiliated to MINATEC R&D center

27 permanent staff members, 16 PhD students and 7 post-docs

Why MRAM ?

	DRAM	SRAM	FLASH	FeRAM	MRAM
Write cycle	50ns	8ns	200µs	80ns	30ns
Read cycle	50ns	8ns	60ns	80ns	30ns
Cell size (F^2)	8-12	50-80	4-11	4-16	6-20
Endurability write/read	∞/∞	∞/∞	10^6/∞	>10^{12}/>10^{12}	>10^{15}/∞
Power consumption	High	Low	Low	Low	Low
Refresh	Yes	No	No	No	No
Retention	No	No	Yes	Partially	Yes
Scalability limits	capacitor	6 transistors	tunnel oxide	capacitor	current density
Write/erase	Charge capacitance	CMOS logic	Charge tunnelling	Ferroelectric	Magnetization

- **Non-Volatility of FLASH**
- **Density competitive with DRAM**
- **Speed competitive with SRAM**

Why Thermally Assisted MRAM ?

Problems in conventional MRAM

Selectivity -> difficulty in writing a single junction

Scalability -> electromigration in magnetic field lines with decreasing in-plane size

Thermal stability -> reduced life-time of written information

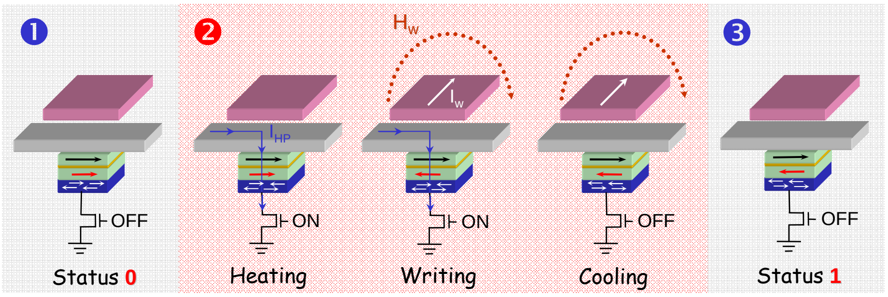
New approaches

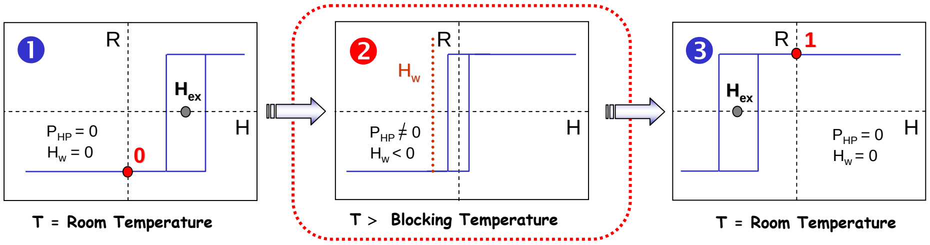
1. **Thermally assisted MRAM** (Spintec Patent + lab. demo)
   - good thermal stability ensured by exchange coupling of the storage layer with an Antiferromagnet;
   - high selectivity;
   - low power consumption during writing at high temperature.
2. **Current induced magnetization switching**
   - linear decrease of power consumption with decreasing junction in-plane area
3. **Possibility to integrate 1 and 2**

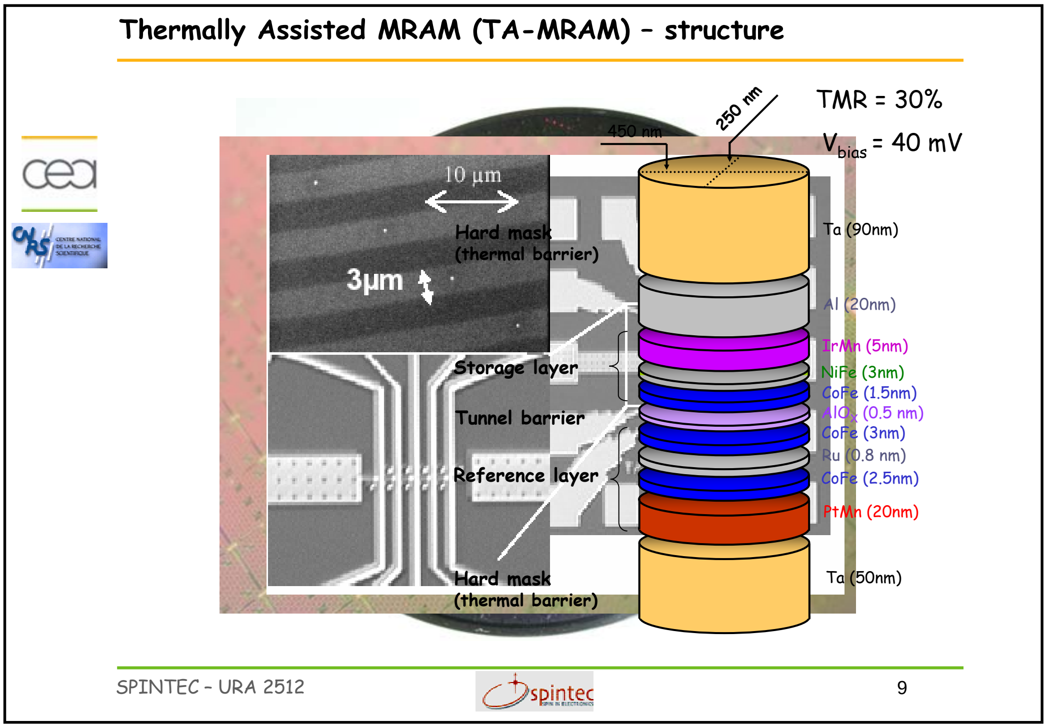
Outline

1. TA-MRAM. Definition, structure and principle of operation.
2. Electric characterization
3. Regimes of operation. Power of the electric pulse P_{HP} *vs.* junction temperature T_{AF}.
4. Exchange bias as a temperature probe. Electric pulse width δ *vs.* junction temperature T_{AF}.
5. Conclusions

Thermally Assisted MRAM (TA-MRAM) – principle







Thermally Assisted MRAM (TA-MRAM) – structure

TMR = 30%

V_{bias} = 40 mV

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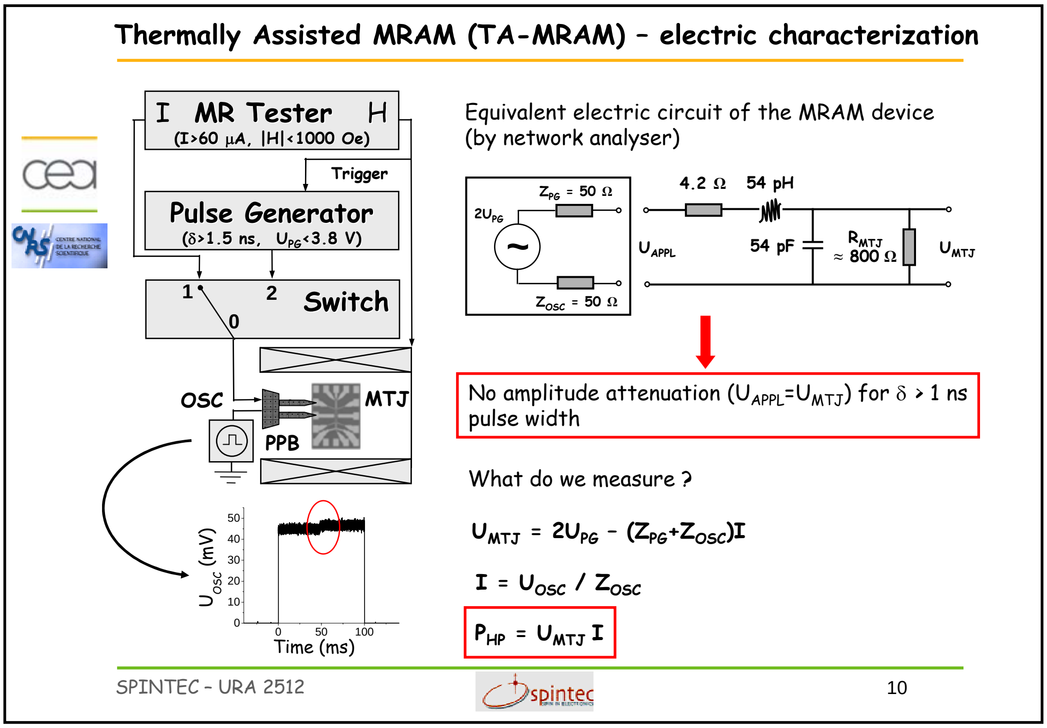

Thermally Assisted MRAM (TA-MRAM) – electric characterization

Equivalent electric circuit of the MRAM device (by network analyser)

No amplitude attenuation ($U_{APPL}=U_{MTJ}$) for $\delta > 1$ ns pulse width

What do we measure ?

$$U_{MTJ} = 2U_{PG} - (Z_{PG}+Z_{OSC})I$$

$$I = U_{OSC} / Z_{OSC}$$

$$\boxed{P_{HP} = U_{MTJ} I}$$

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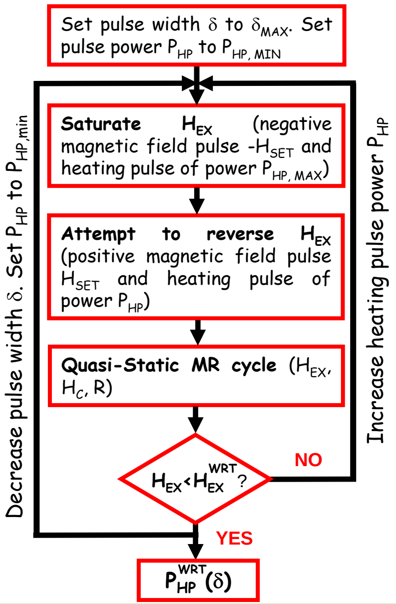
Thermally Assisted MRAM (TA-MRAM) – measurement procedure



Set pulse width δ to δ_{MAX}. Set pulse power P_{HP} to $P_{HP,\,MIN}$

Saturate H_{EX} (negative magnetic field pulse $-H_{SET}$ and heating pulse of power $P_{HP,\,MAX}$)

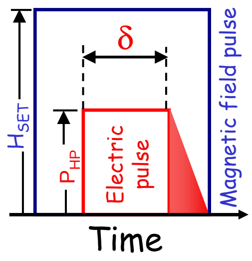
Attempt to reverse H_{EX} (positive magnetic field pulse H_{SET} and heating pulse of power P_{HP})

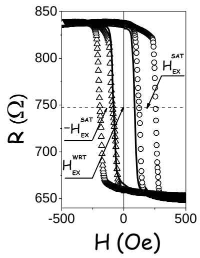
Quasi-Static MR cycle (H_{EX}, H_C, R)

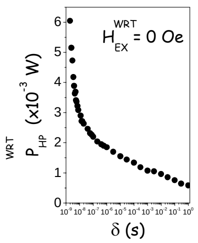
$H_{EX} < H_{EX}^{WRT}$?

$P_{HP}^{WRT}(\delta)$

How do we measure ?

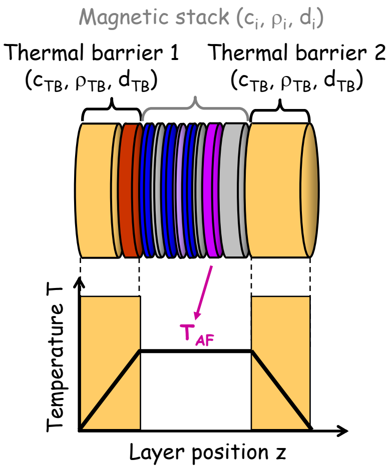






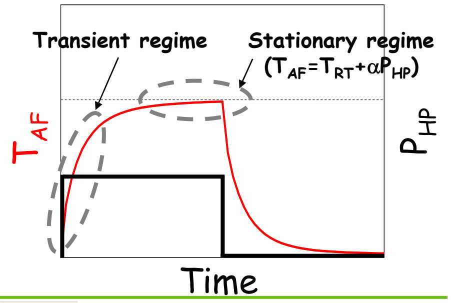
Thermally Assisted MRAM (TA-MRAM) – operation regimes

1-D model of heat diffusion in the MTJ stack

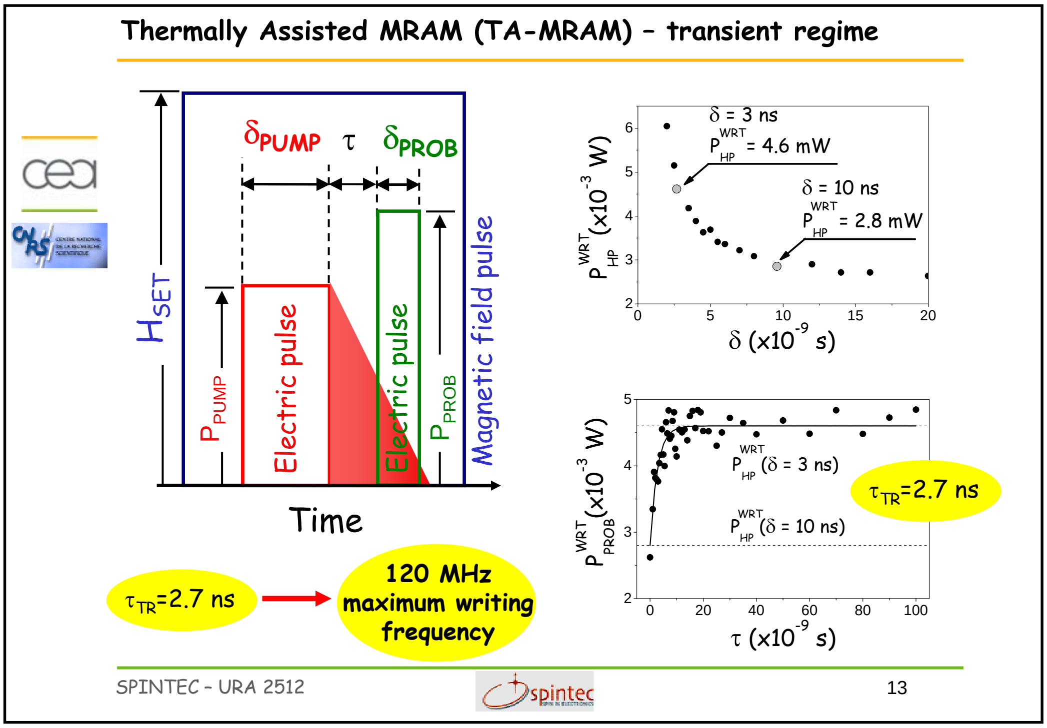


$$\left(\sum_i c_i\rho_i d_i + c_{TB}\rho_{TB}d_{TB}\right)\frac{\partial T}{\partial t} - 2\frac{k_{TB}}{d_{TB}}\left(T - T_{RT}\right) = \frac{P_{HP}}{S}$$

$$\boxed{\begin{aligned} T_{AF} &= T_{RT} + \alpha P_{HP}\left[1 - \exp\left(-\frac{t}{\tau_{TR}}\right)\right] \\ \tau_{TR} &= \frac{d_{TB}}{2k_{TB}}\left(\sum_i c_i\rho_i d_i + c_{TB}\rho_{TB}d_{TB}\right) \\ \alpha &= \frac{d_{TB}}{2k_{TB}S} \end{aligned}}$$

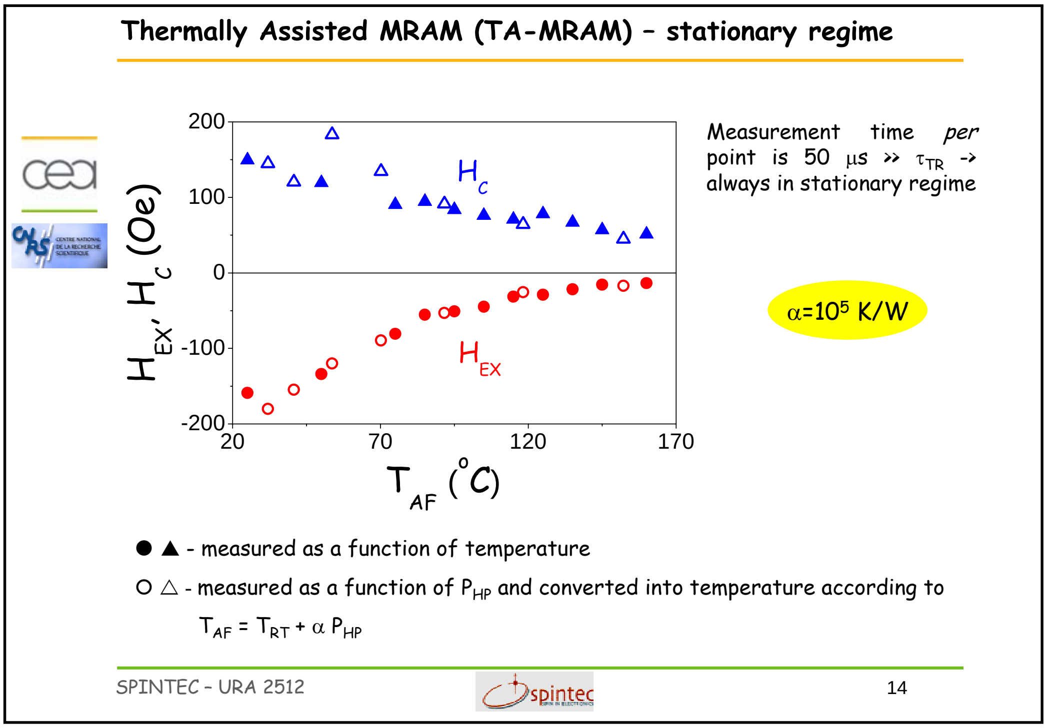


c – specific heat capacity J/(Kg K)
k – thermal conductivity W/(K m)
ρ – density Kg/m³
d – layer thickness m



Thermally Assisted MRAM (TA-MRAM) – transient regime

τ_{TR}=2.7 ns → **120 MHz maximum writing frequency**



Thermally Assisted MRAM (TA-MRAM) – stationary regime

Measurement time *per* point is 50 μs >> τ_{TR} -> always in stationary regime

$\alpha = 10^5$ K/W

● ▲ - measured as a function of temperature

○ △ - measured as a function of P_{HP} and converted into temperature according to

$T_{AF} = T_{RT} + \alpha P_{HP}$

Thermally Assisted MRAM (TA-MRAM) – consistency of results

Material	ρ kg/m³	c* J/(K kg)	k** W/(K m)
Ta*** (β)	16327	144	4.3
PtMn	12479	247	4.9
CoFe	8658	446	37
Ru	12370	239	120
AlOx	3900	900	27
IrMn	10181	316	5.7
NiFe	8694	447	37
Al	2700	904	235
SiO_2	2200	730	1.4

*for metallic alloys calculated according to Dulong-Petit law

**for metallic alloys calculated according to Widemann-Franz law

***confirmed by electrical resistivity measurements (170 μΩxcm) and XRD scan

Theory – 1D model of heat diffusion

ρ_{TB} = 15846 kg/m³

c_{TB} = 154.1 J/(K kg)

k_{TB} = 4.38 W/(K m)

$$\sum_i c_i \rho_i d_i + c_{TB}\rho_{TB}d_{TB} = 0.306 \ \ \mathrm{J/(K\,m^2)}$$

Experiment

($\alpha = 10^5$ K/W, τ_{TR} = 2.7 ns)

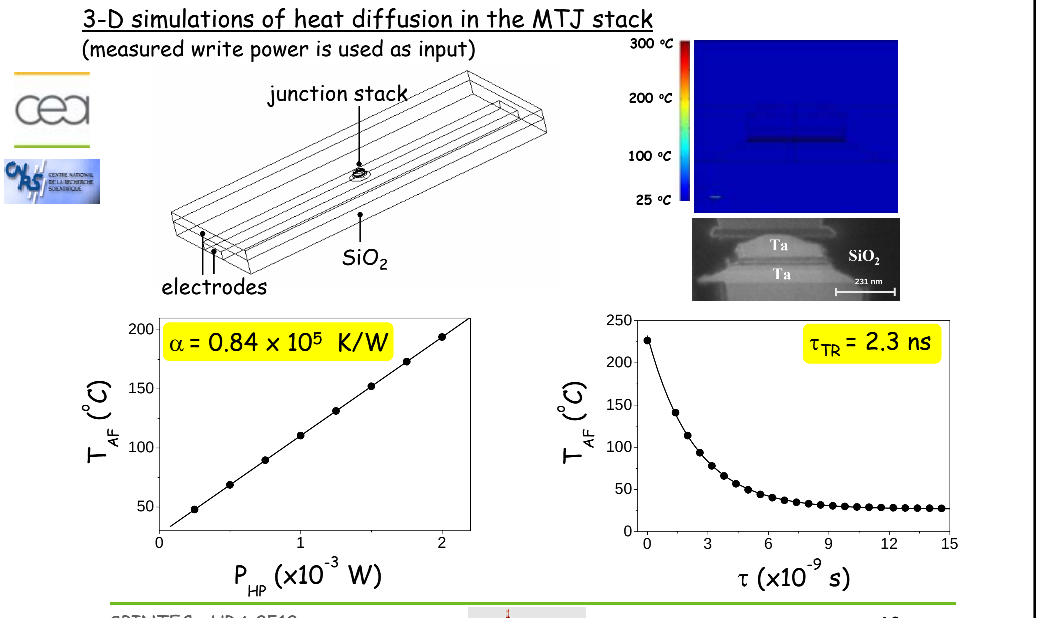
$$k_{TB} = d_{TB}/(2\alpha S) = 4.53 \ \mathrm{W/(K\,m)}$$

$$\sum_i c_i \rho_i d_i + c_{TB}\rho_{TB}d_{TB} = \tau_{TR}/(\alpha S) = 0.315 \ \ \mathrm{J/(K\,m^2)}$$

Thermally Assisted MRAM (TA-MRAM) – consistency of results

3-D simulations of heat diffusion in the MTJ stack

(measured write power is used as input)



Thermally Assisted MRAM (TA-MRAM) – conclusions

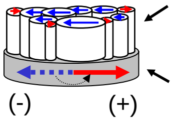
✓ Two temperature regimes of the MTJ evidenced:

- ➢ transient temperature regime for pulse widths $\delta < 9$ ns;
- ➢ stationary temperature regime for longer pulse widths; in this regime, the relationship between the temperature of the storage layer T_{AF} and the power of the electric pulse P_{HP} is linear: $T_{AF} = T_{RT} + 10^5\ (K/W)\ P_{HP}$.

✓ Use of thermal barrier layers reduces the electric power density required for writing but also decreases the writing frequency

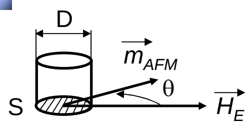
✓ The writing power density increases with decreasing pulse width from 0.6 mW for δ = 1 s up to 6 mW for δ = 2 ns; even in the range of pulse widths 1 s - 10 ns, where the storage layer reaches the stationary temperature regime by the end of the electric pulse, the writing power shows a 500 % increase.

Thermally Assisted MRAM (TA-MRAM) – exchange bias as temperature probe



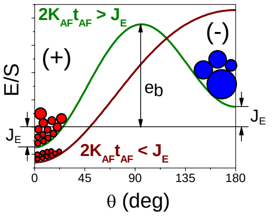
AFM layer = collection of non-interacting single domain grains

FM layer = single domain



$$m_{AF} = \mu_{AF} D / a_0$$
$$H_E = J_{INT} / \mu_{AF}$$
$$J_{INT} = J_0 \mu_F \mu_{AF}$$

$$E/S = K_{AF} t_{AF} \sin^2\theta - J_E \cos\theta$$



$$J_E = J_{INT} / (a_0 D)$$

$$p_+(t) = p_+^{eq}\left(1 - e^{-t/\tau}\right) + p_+^{ini} e^{-t/\tau}$$

$$p_+^{eq} = 1/\left[1 + e^{2J_E S/(k_B T)}\right]$$

$$\frac{1}{\tau} = f_0\left[e^{-(e_b - J_E)S/(k_B T)} + e^{-(e_b + J_E)S/(k_B T)}\right]$$

$$e_b = K_{AF} t_{AF}\left[1 + 1/4\left(J_E / K_{AF} t_{AF}\right)^2\right]$$

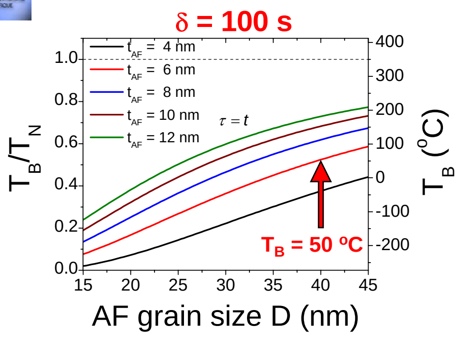
Thermally Assisted MRAM (TA-MRAM) – exchange bias as temperature probe

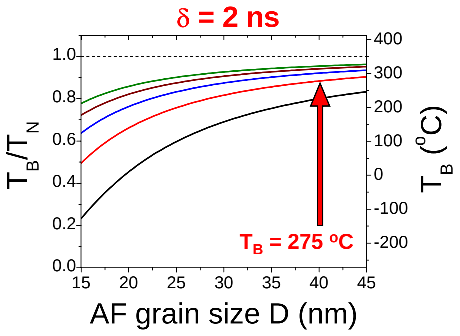
$Ni_{80}Fe_{20}/Ir_{20}Mn_{80}$ Ferromagnetic/Antiferromagnetic bilayer

$$\begin{cases} T_{Neel}=350\ ^{o}C,\ a_0=2.7\ \text{Å},\ \lambda=0.33 \\ J_{INT} = 8.11\times10^{-15}\ \text{erg} \\ K_{AF} = 2.44\times10^{5}\ \text{erg/cm}^3 \end{cases}$$

$$\boxed{\tau\big|_{T=T_B} = \delta}$$

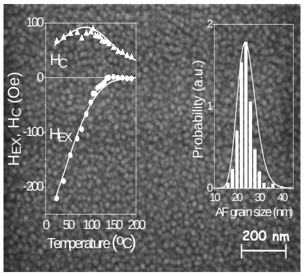
R.White et al, J.Appl.Phys. 92, 4828 (2002)





Decreasing the pulse width δ may require a considerable increase of the writing temperature !!!

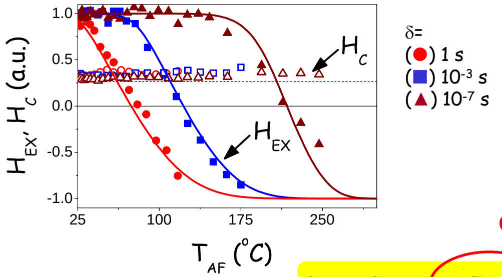
Thermally Assisted MRAM (TA-MRAM) – exchange bias as temperature probe



K_{AF} = 7.3 x 10^5 erg/cm^3

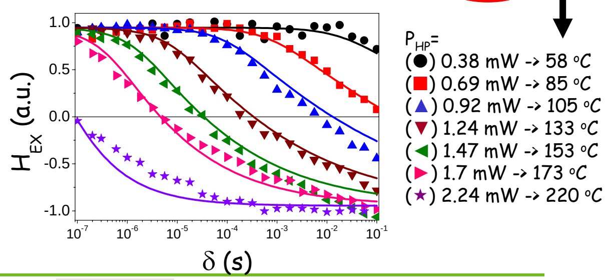
K_F = 1.3 x 10^4 erg/cm^3

J_{INT} = 8.5 x 10^{-15} erg

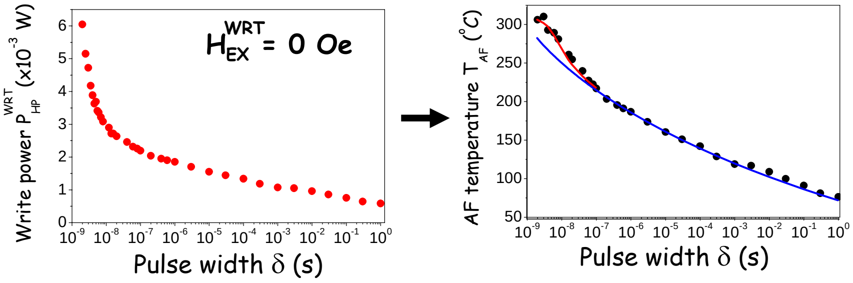


α

$T_{AF} = T_{RT} + 8.97\times10^3\ P_{HP}$



Thermally Assisted MRAM (TA-MRAM) – exchange bias as temperature probe



● 3-D simulation of heat diffusion – experimental write power $P_{HP}^{WRT}(\delta)$ is used as input

🟦 Exchange bias model - temperature required to set $H_{EX}^{WRT} = 0$ for heating time equal to the pulse duration δ; temperature pulse shape is assumed rectangular.

🟥 Exchange bias model - temperature required to set $H_{EX}^{WRT} = 0$ for heating time equal to the pulse duration δ; temperature pulse shape is calculated by 3-D simulation of heat diffusion.

Conclusion

✓ Writing temperature increases with decreasing pulse width δ as a consequence of thermal relaxation in the Antiferromagnetic storage layer and approaches the Neel temperature in the limit δ -> 0.

Exemple: writing with 2 ns pulses imply heating at about 300 °C with possible negative effects on the integrity of tunnel barrier and storage layer antiferromagnet.

Solution: decrease the writing temperature by using antiferromagnets of lower Nèel temperature than IrMn ($T_N \approx 350$ °C) for pinning the storage layer.