Content

- **Scaling**
- **More Moore**
  - **Lithography**
  - **Transistor scaling**
  - **Interconnect**
  - **Power**
- **More than Moore**
- **Manufacturing**
- **Conclusions**

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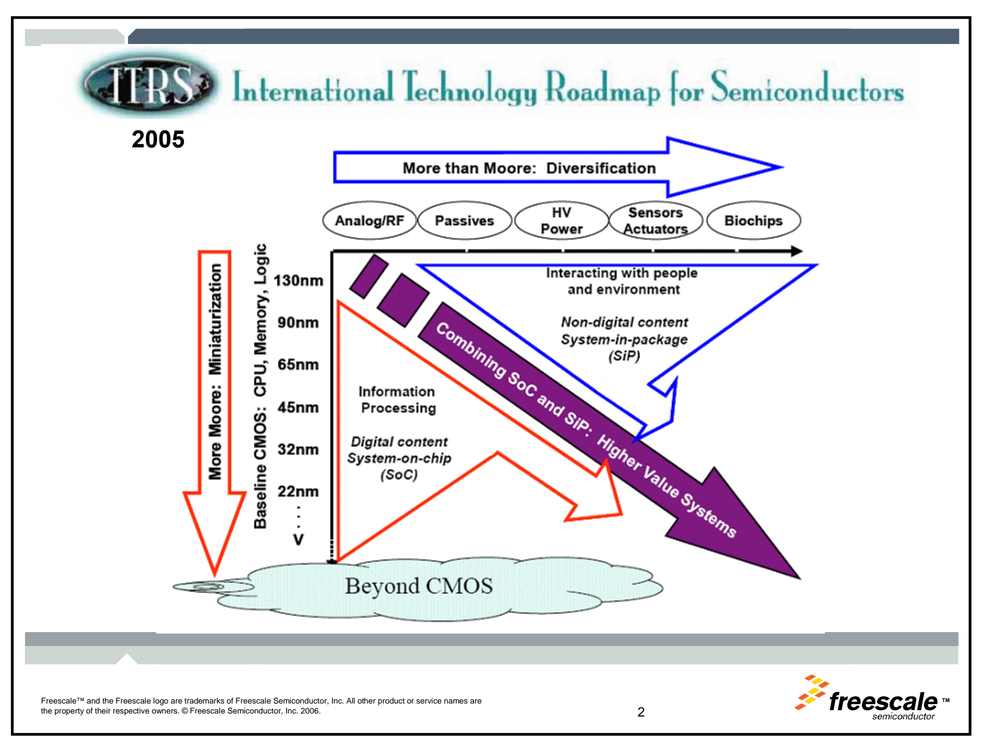

International Technology Roadmap for Semiconductors
2005
More than Moore: Diversification
Analog/RF
Passives
HV Power
Sensors Actuators
Biochips
More Moore: Miniaturization
Baseline CMOS: CPU, Memory, Logic
130nm
90nm
65nm
45nm
32nm
22nm
Interacting with people and environment
Non-digital content System-in-package (SiP)
Information Processing
Digital content System-on-chip (SoC)
Combining SoC and SiP: Higher Value Systems
Beyond CMOS
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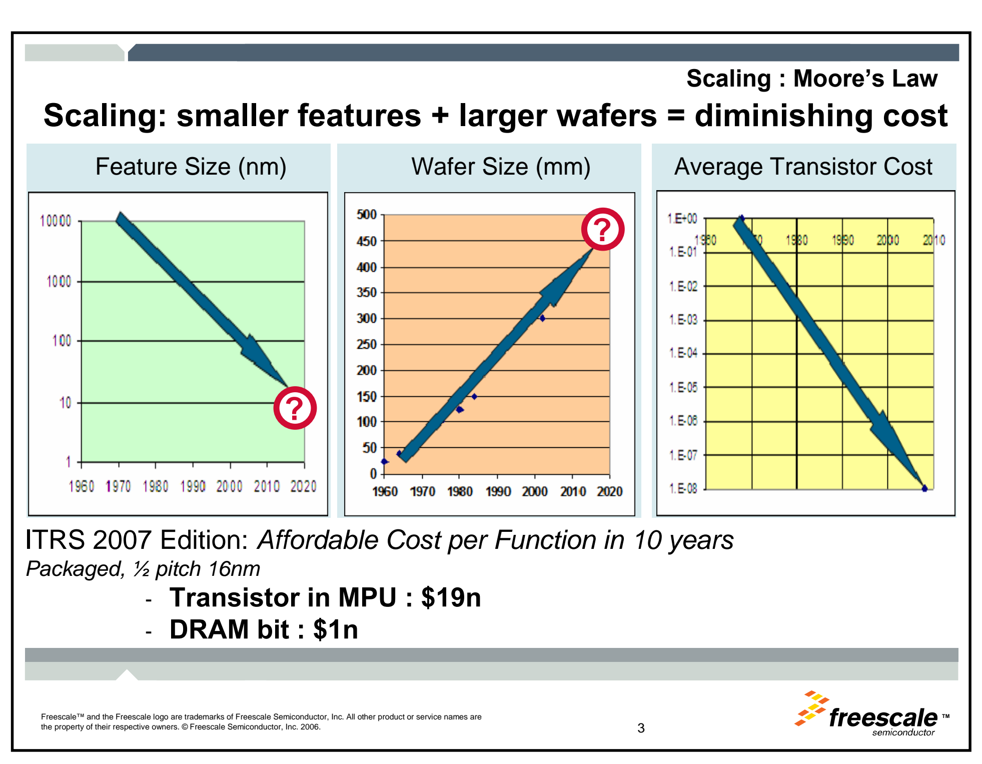

Scaling : Moore's Law
Scaling: smaller features + larger wafers = diminishing cost
Feature Size (nm)
Wafer Size (mm)
Average Transistor Cost
ITRS 2007 Edition: Affordable Cost per Function in 10 years
Packaged, ½ pitch 16nm
- Transistor in MPU : $19n
- DRAM bit : $1n
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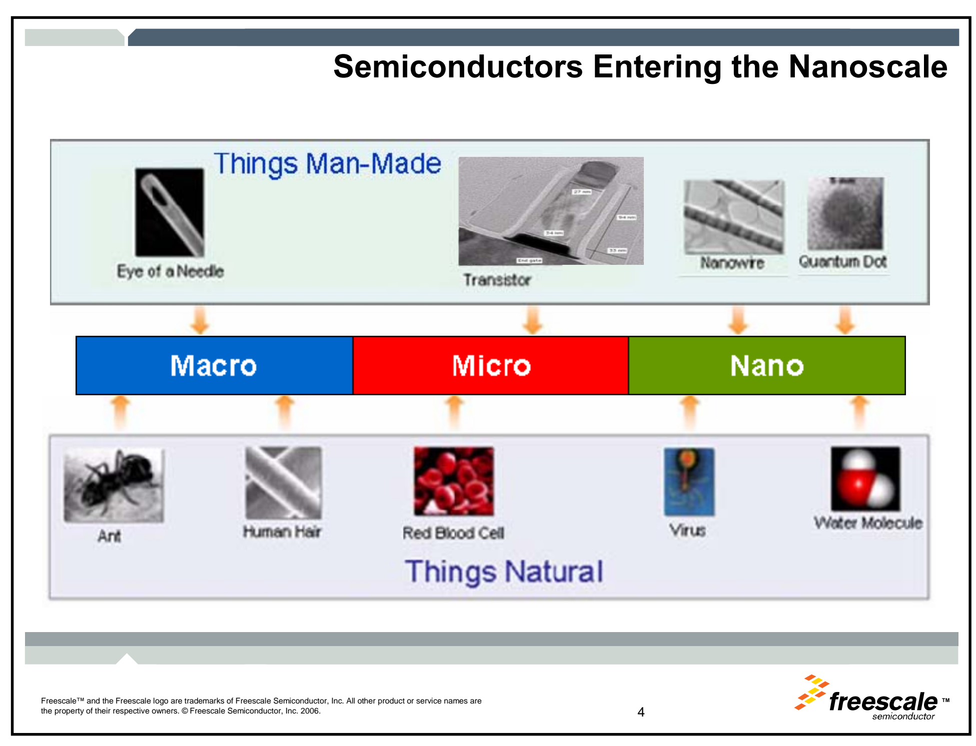

Semiconductors Entering the Nanoscale
Things Man-Made
Eye of a Needle
Transistor
Nanowire
Quantum Dot
Macro
Micro
Nano
Ant
Human Hair
Red Blood Cell
Virus
Water Molecule
Things Natural
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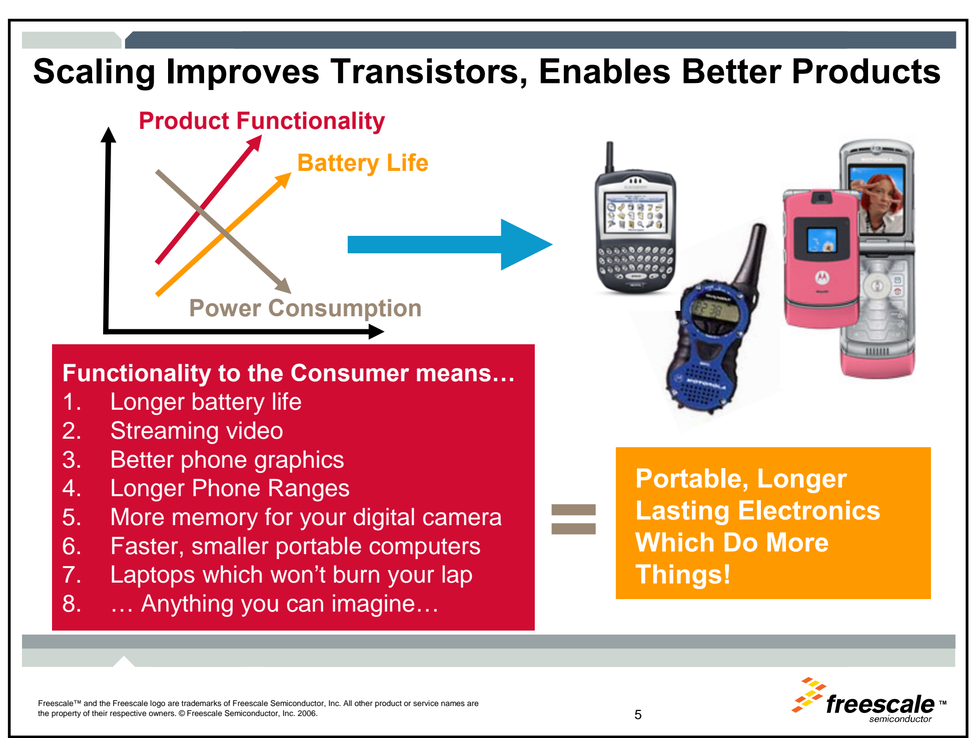

Scaling Improves Transistors, Enables Better Products
Product Functionality
Battery Life
Power Consumption
Functionality to the Consumer means…
1. Longer battery life
2. Streaming video
3. Better phone graphics
4. Longer Phone Ranges
5. More memory for your digital camera
6. Faster, smaller portable computers
7. Laptops which won't burn your lap
8. … Anything you can imagine…
=
Portable, Longer Lasting Electronics Which Do More Things!
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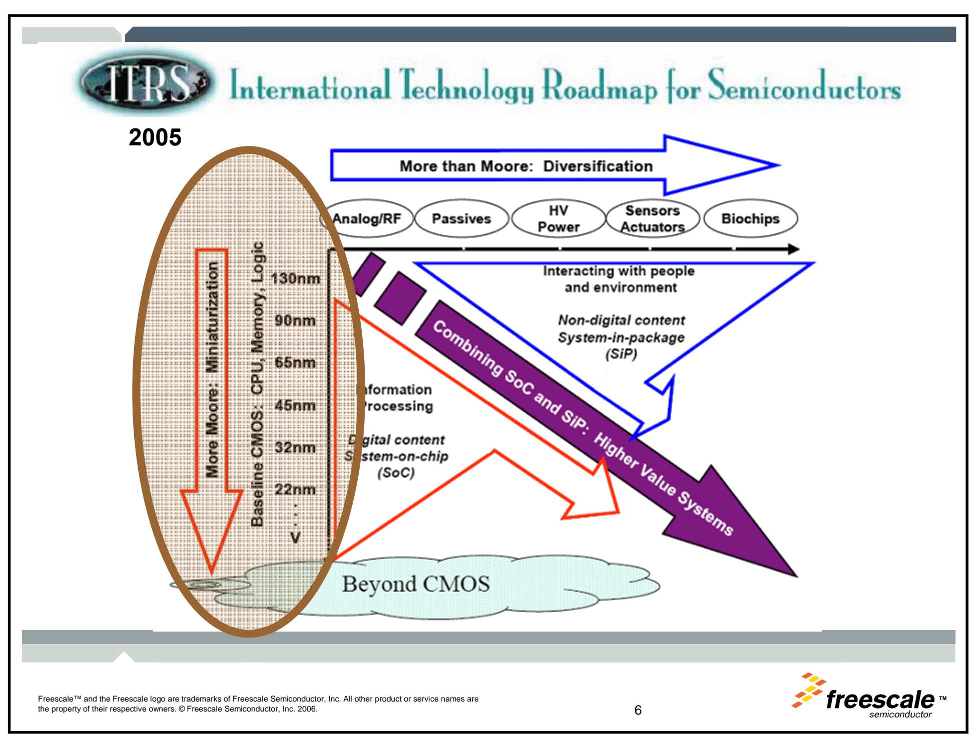

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45nm
32nm
22nm
V
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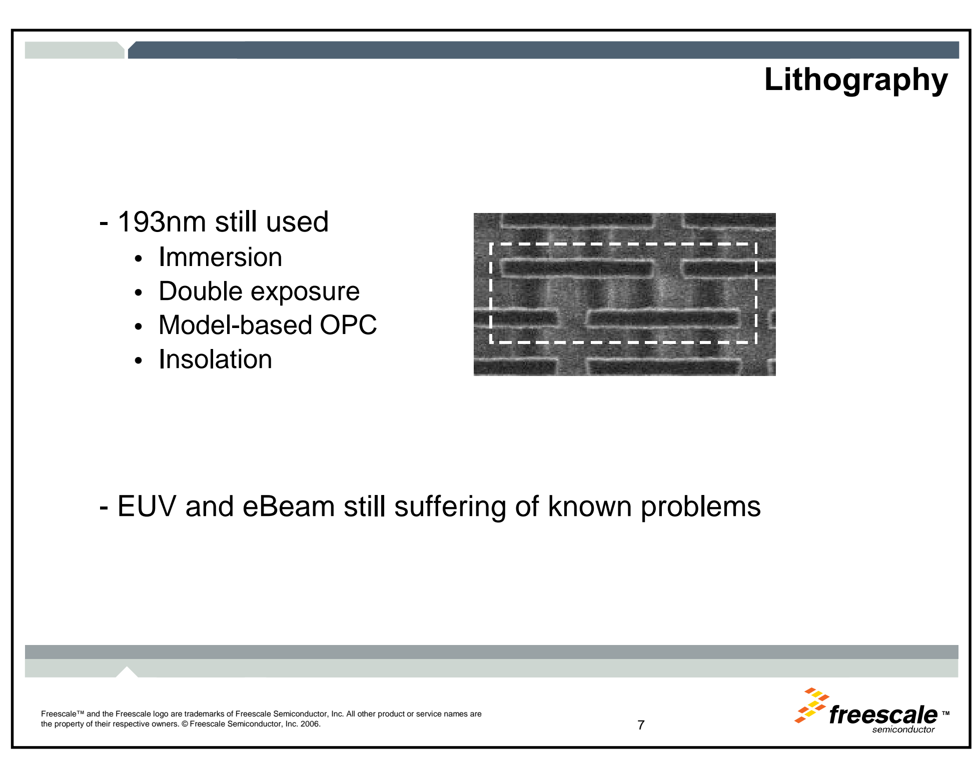

Lithography
- 193nm still used
• Immersion
• Double exposure
• Model-based OPC
• Insolation
- EUV and eBeam still suffering of known problems
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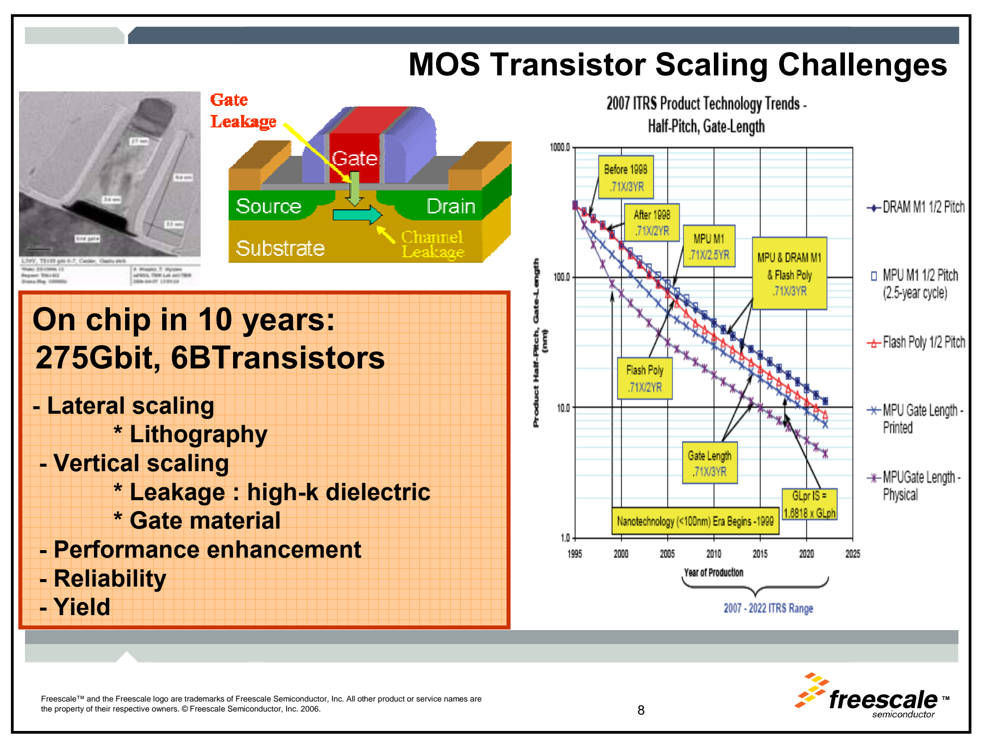
MOS Transistor Scaling Challenges
Gate Leakage
Gate
Source
Drain
Substrate
Channel Leakage
On chip in 10 years:
275Gbit, 6BTransistors
- Lateral scaling
* Lithography
- Vertical scaling
* Leakage : high-k dielectric
* Gate material
- Performance enhancement
- Reliability
- Yield
2007 ITRS Product Technology Trends - Half-Pitch, Gate-Length
Before 1998 .71X/3YR
After 1998 .71X/2YR
MPU M1 .71X/2.5YR
MPU & DRAM M1 & Flash Poly .71X/3YR
Flash Poly .71X/2YR
Gate Length .71X/3YR
GLpr IS = 1.6818 x GLph
Nanotechnology (<100nm) Era Begins -1999
Product Half-Pitch, Gate-Length (nm)
Year of Production
2007 - 2022 ITRS Range
DRAM M1 1/2 Pitch
MPU M1 1/2 Pitch (2.5-year cycle)
Flash Poly 1/2 Pitch
MPU Gate Length - Printed
MPUGate Length - Physical
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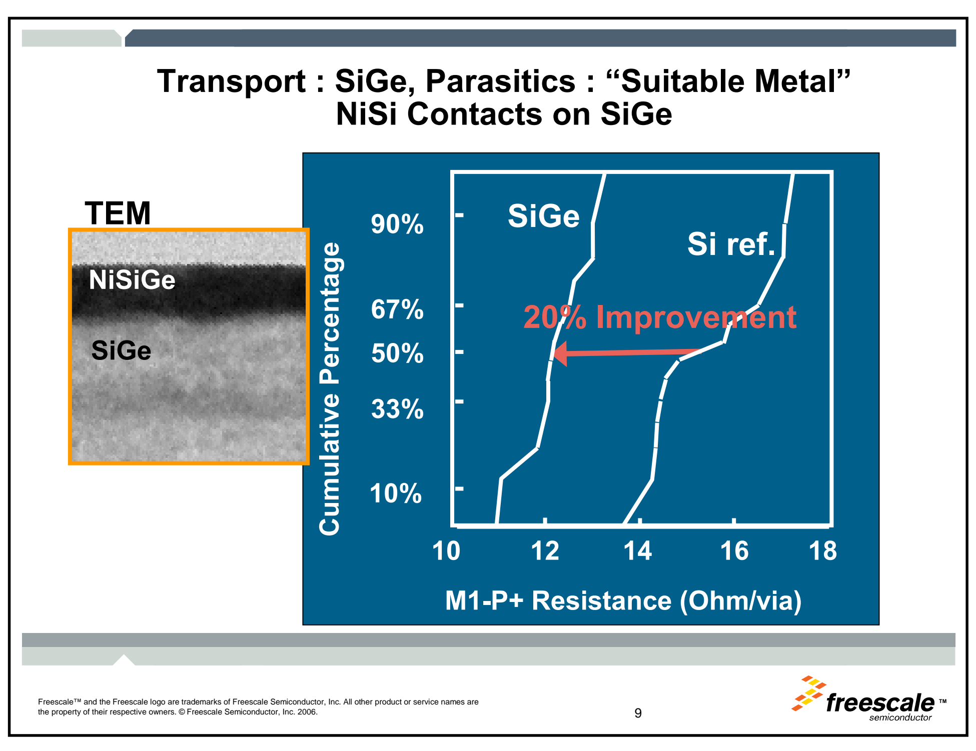
Transport : SiGe, Parasitics : “Suitable Metal”
NiSi Contacts on SiGe
TEM
NiSiGe
SiGe
Cumulative Percentage
90%
67%
50%
33%
10%
SiGe
Si ref.
20% Improvement
10
12
14
16
18
M1-P+ Resistance (Ohm/via)
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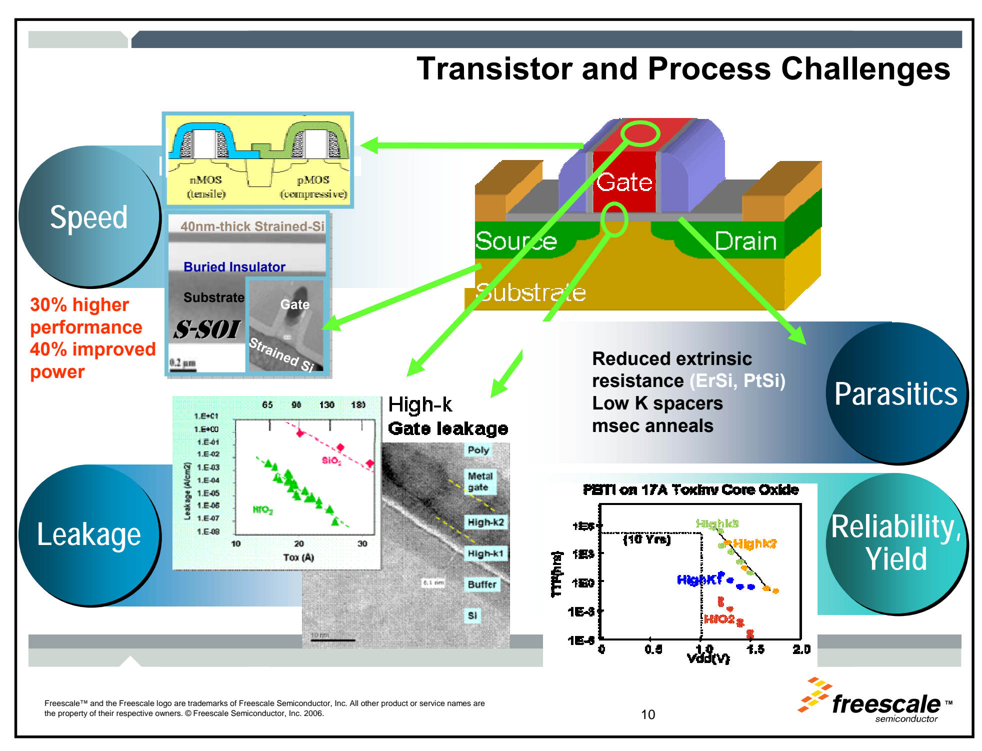

Transistor and Process Challenges
Speed
nMOS (tensile)
pMOS (compressive)
40nm-thick Strained-Si
Buried Insulator
Substrate
S-SOI
Gate
Strained Si
30% higher performance
40% improved power
Gate
Source
Drain
Substrate
High-k
Gate leakage
Poly
Metal gate
High-k2
High-k1
Buffer
Si
Tox (A)
Reduced extrinsic resistance (ErSi, PtSi)
Low K spacers
msec anneals
Parasitics
Leakage
PBTI on 17A Toxinv Core Oxide
Vdd(V)
Reliability, Yield
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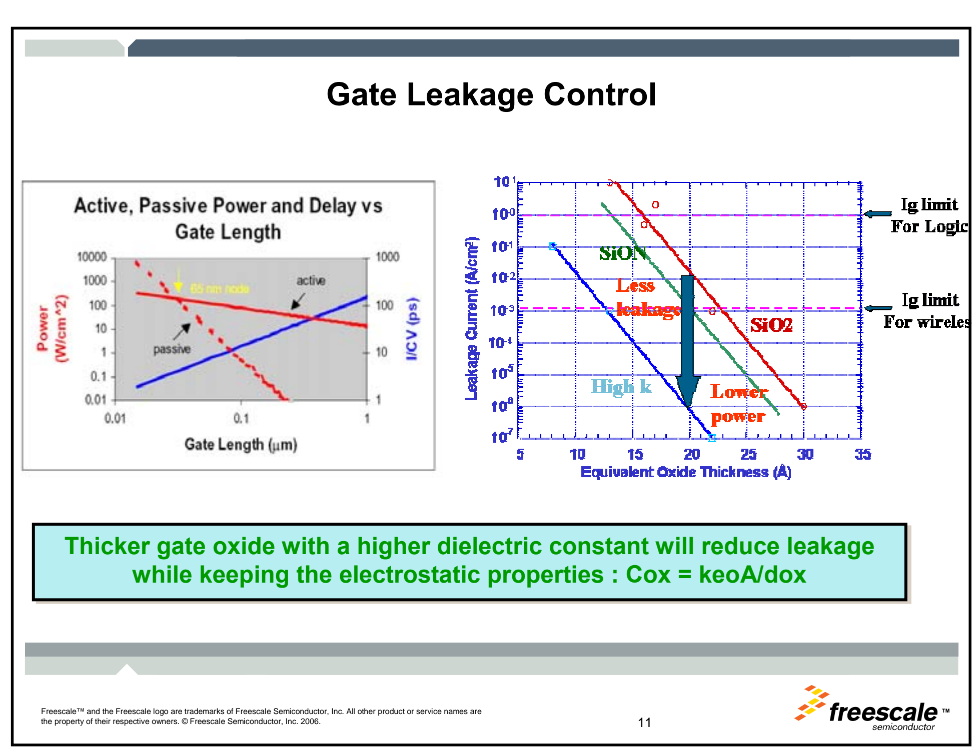

Gate Leakage Control
Active, Passive Power and Delay vs Gate Length
Power (W/cm^2)
I/CV (ps)
active
passive
Gate Length (μm)
Leakage Current (A/cm²)
Ig limit For Logic
Ig limit For wireles
SiON
Less leakage
SiO2
High k
Lower power
Equivalent Oxide Thickness (Å)
Thicker gate oxide with a higher dielectric constant will reduce leakage while keeping the electrostatic properties : Cox = keoA/dox
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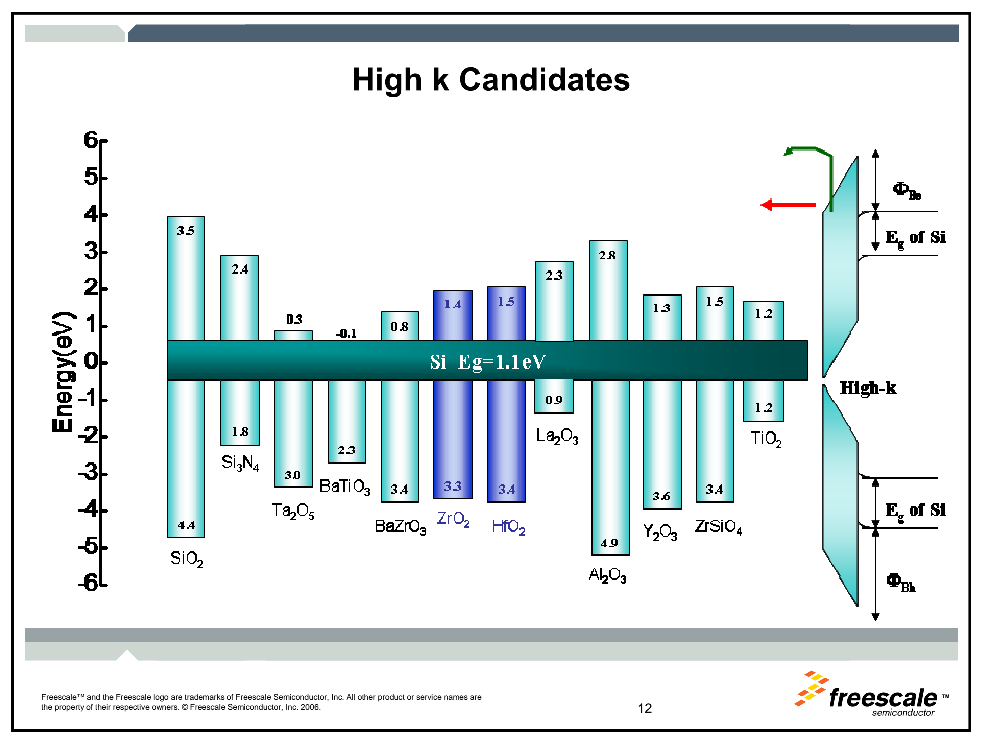
High k Candidates
Energy(eV)
Si Eg=1.1eV
SiO2
Si3N4
Ta2O5
BaTiO3
BaZrO3
ZrO2
HfO2
La2O3
Al2O3
Y2O3
ZrSiO4
TiO2
High-k
Eg of Si
Eg of Si
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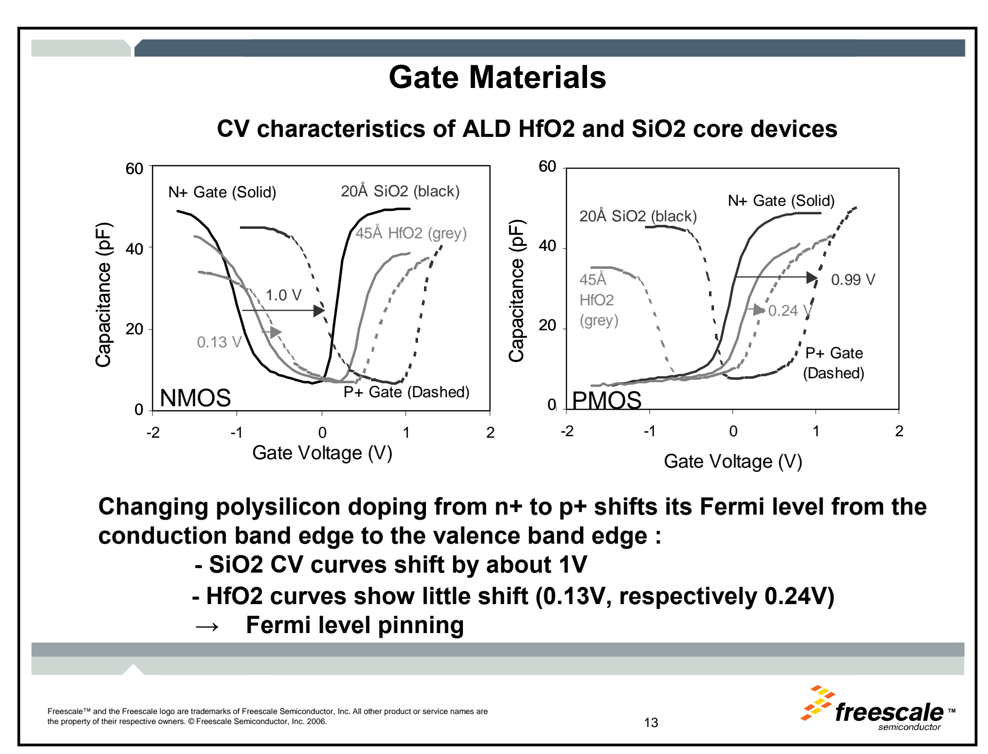
Gate Materials
CV characteristics of ALD HfO2 and SiO2 core devices
N+ Gate (Solid)
20Å SiO2 (black)
45Å HfO2 (grey)
1.0 V
0.13 V
NMOS
P+ Gate (Dashed)
Capacitance (pF)
Gate Voltage (V)
20Å SiO2 (black)
N+ Gate (Solid)
45Å HfO2 (grey)
0.99 V
0.24 V
P+ Gate (Dashed)
PMOS
Capacitance (pF)
Gate Voltage (V)
Changing polysilicon doping from n+ to p+ shifts its Fermi level from the conduction band edge to the valence band edge :
- SiO2 CV curves shift by about 1V
- HfO2 curves show little shift (0.13V, respectively 0.24V)
→ Fermi level pinning
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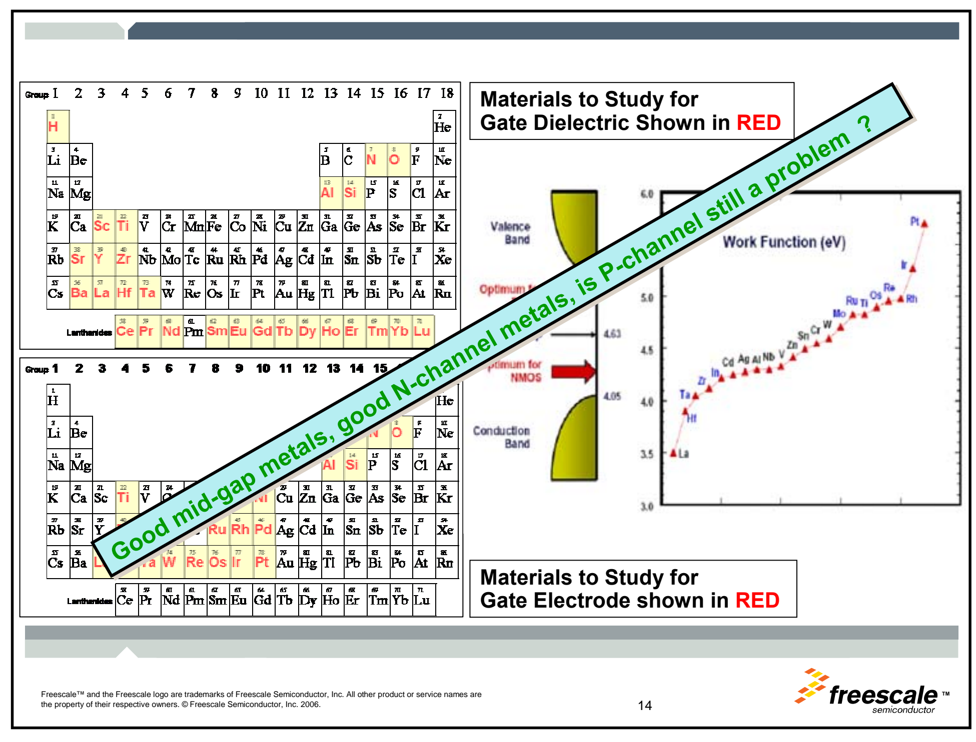
Materials to Study for
Gate Dielectric Shown in RED
Good mid-gap metals, good N-channel metals, is P-channel still a problem ?
Valence Band
Conduction Band
Work Function (eV)
Materials to Study for
Gate Electrode shown in RED
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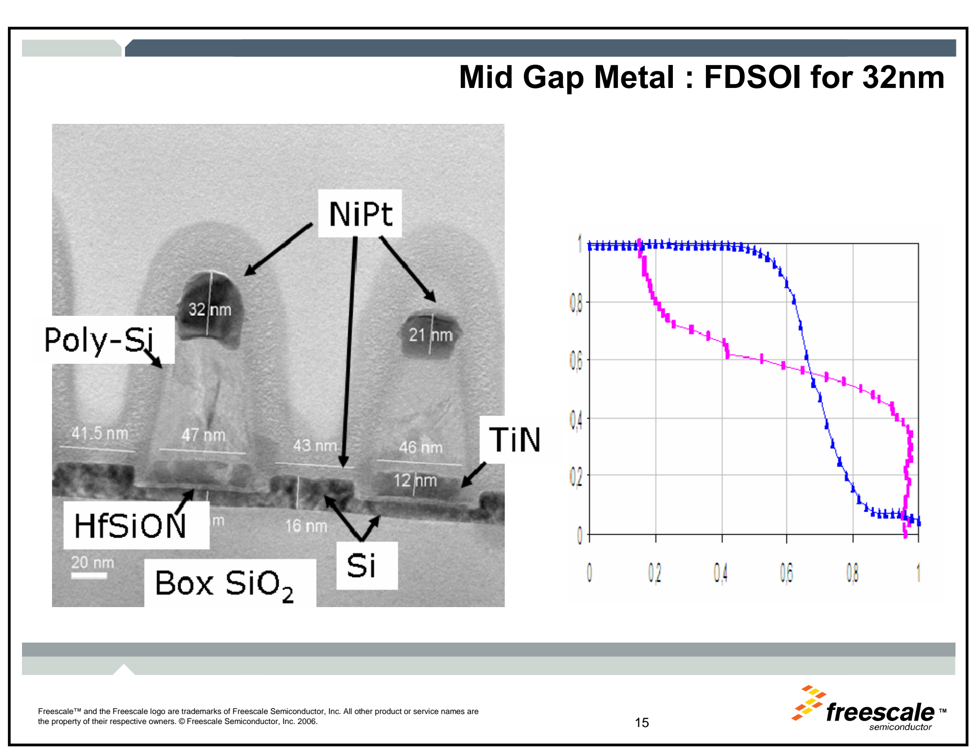
Mid Gap Metal : FDSOI for 32nm
NiPt
Poly-Si
TiN
HfSiON
Box SiO2
Si
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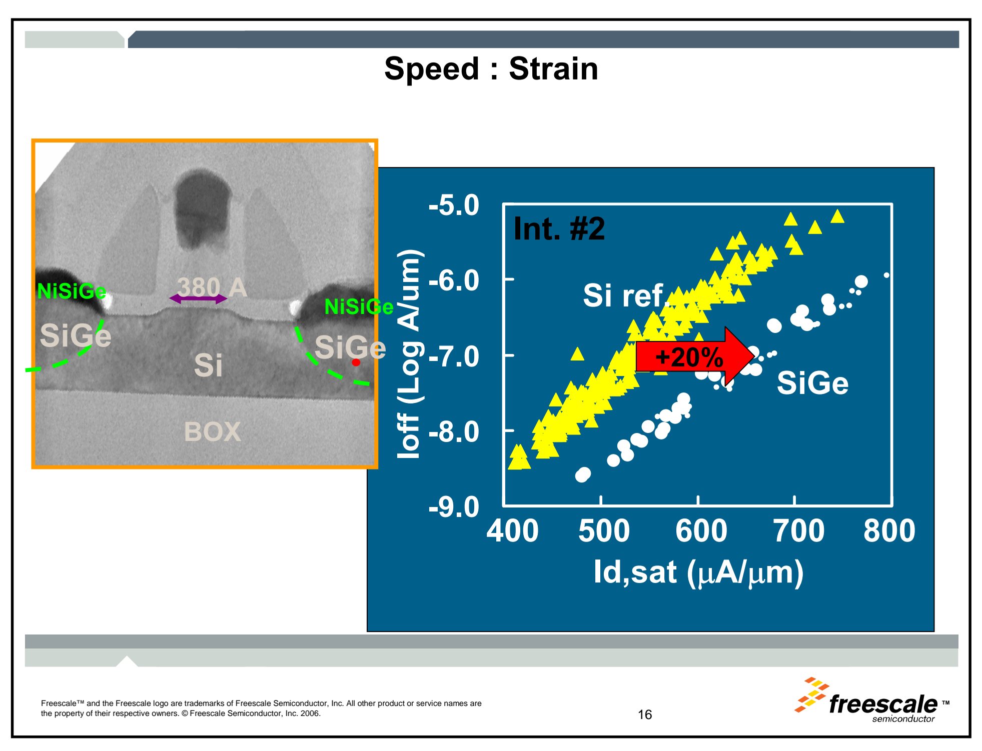
Speed : Strain
NiSiGe
380 A
NiSiGe
SiGe
Si
SiGe
BOX
Int. #2
Si ref
+20%
SiGe
Ioff (Log A/um)
-5.0
-6.0
-7.0
-8.0
-9.0
400
500
600
700
800
Id,sat (μA/μm)
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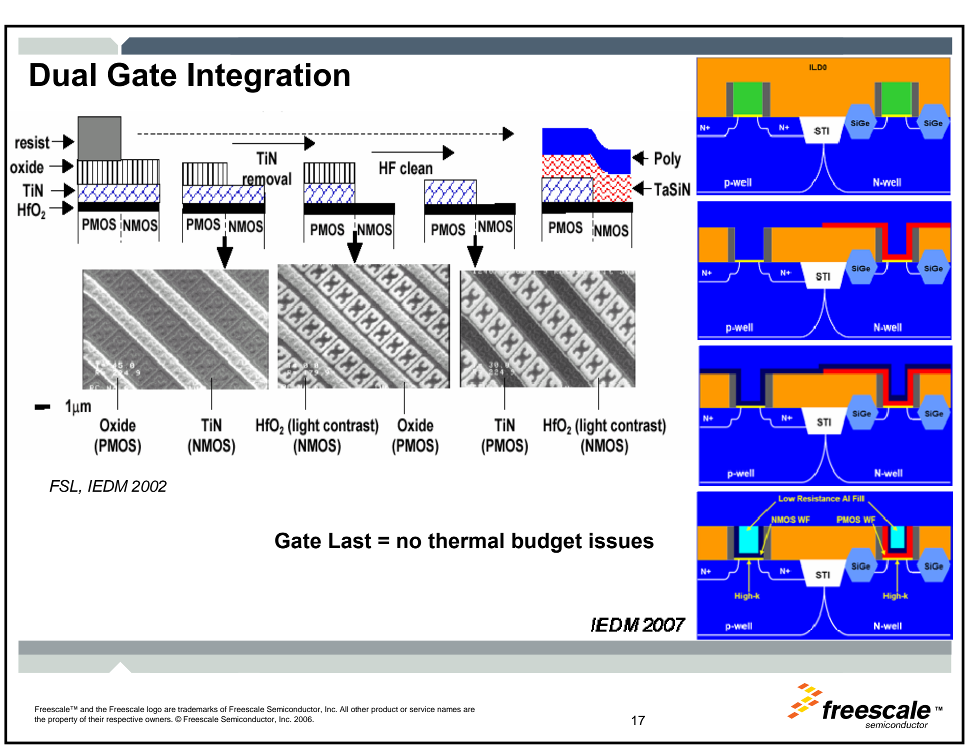
Dual Gate Integration
resist
oxide
TiN
HfO2
PMOS NMOS
TiN removal
HF clean
Poly
TaSiN
1μm
Oxide (PMOS)
TiN (NMOS)
HfO2 (light contrast) (NMOS)
Oxide (PMOS)
TiN (PMOS)
HfO2 (light contrast) (NMOS)
FSL, IEDM 2002
Gate Last = no thermal budget issues
IEDM 2007
ILD0
STI
SiGe
p-well
N-well
Low Resistance Al Fill
NMOS WF
PMOS WF
High-k
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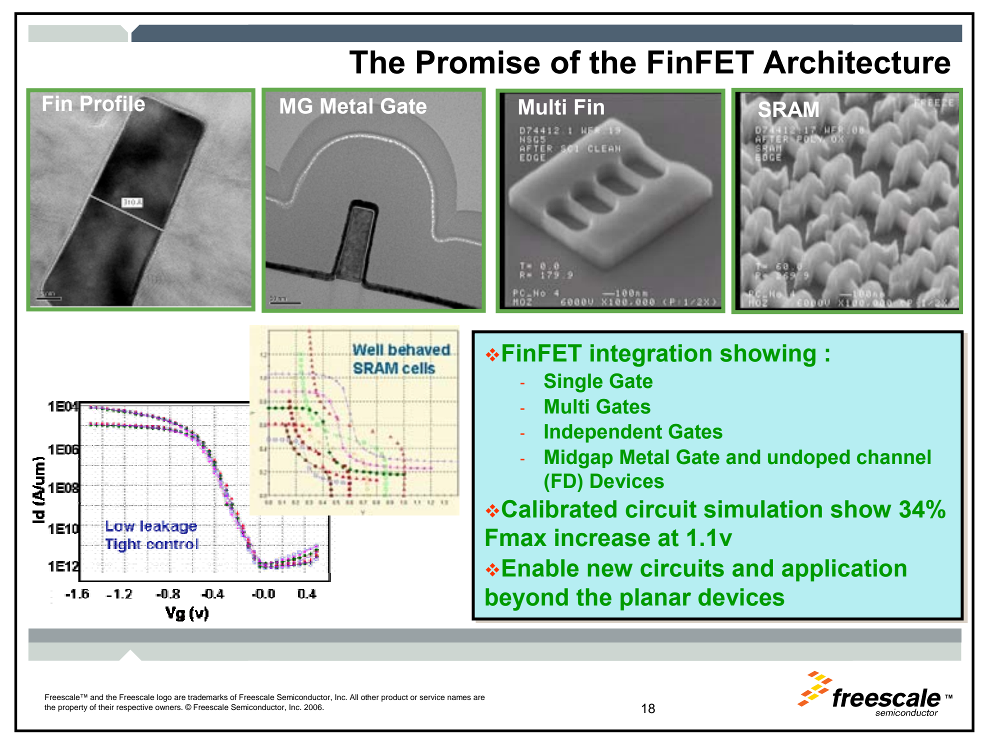
The Promise of the FinFET Architecture
Fin Profile
MG Metal Gate
Multi Fin
SRAM
Well behaved
SRAM cells
Low leakage
Tight control
Id (A/um)
Vg (v)
FinFET integration showing :
- Single Gate
- Multi Gates
- Independent Gates
- Midgap Metal Gate and undoped channel (FD) Devices
Calibrated circuit simulation show 34% Fmax increase at 1.1v
Enable new circuits and application beyond the planar devices
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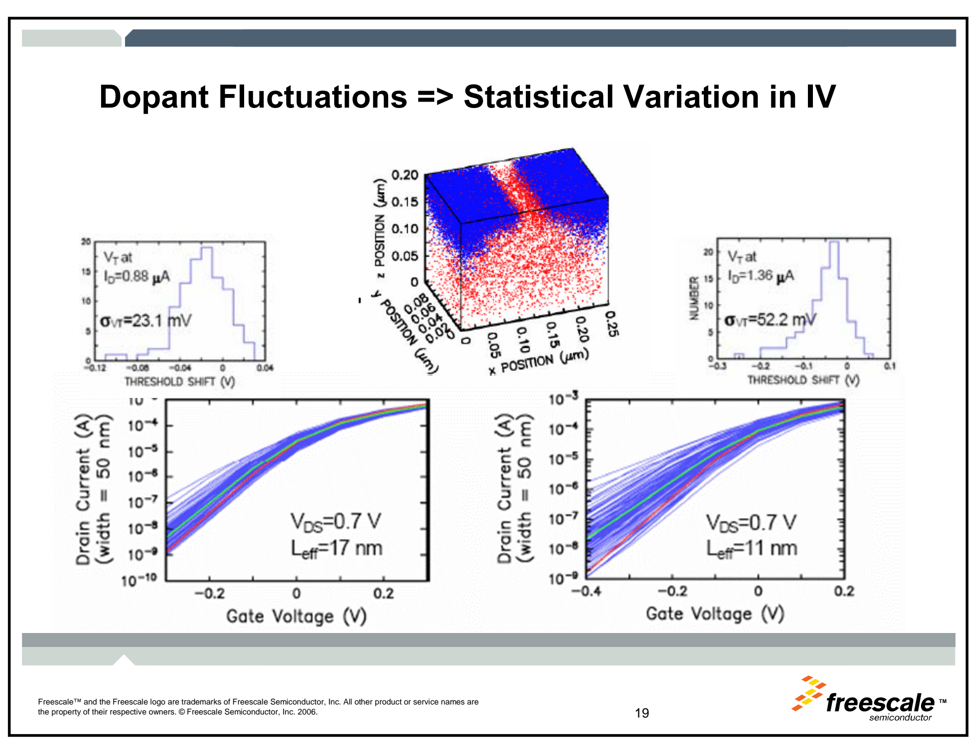
Dopant Fluctuations => Statistical Variation in IV
THRESHOLD SHIFT (V)
NUMBER
z POSITION (μm)
y POSITION (μm)
x POSITION (μm)
Drain Current (A) (width = 50 nm)
Gate Voltage (V)
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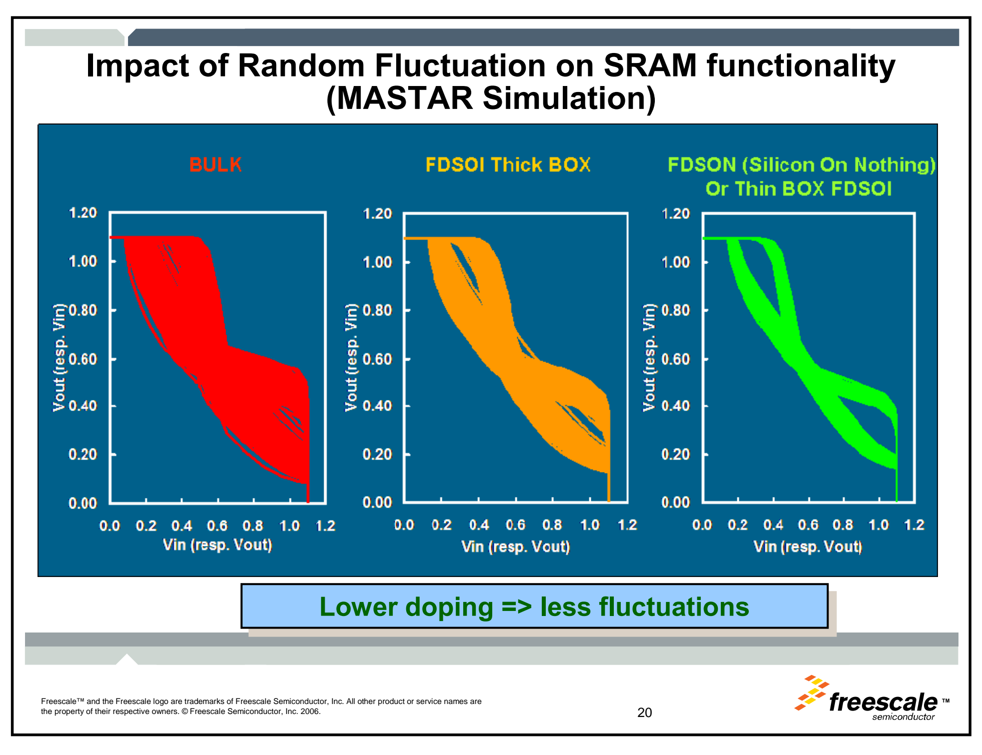
Impact of Random Fluctuation on SRAM functionality
(MASTAR Simulation)
BULK
FDSOI Thick BOX
FDSON (Silicon On Nothing)
Or Thin BOX FDSOI
Vout (resp. Vin)
Vin (resp. Vout)
Lower doping => less fluctuations
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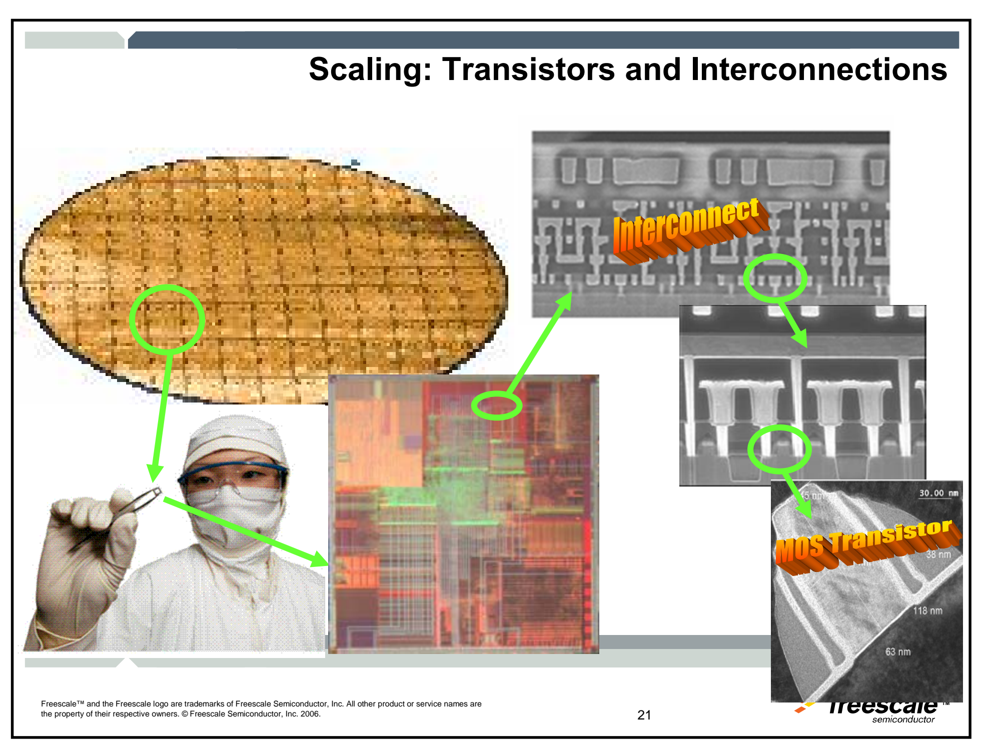
Scaling: Transistors and Interconnections
Interconnect
MOS Transistor
30.00 nm
118 nm
63 nm
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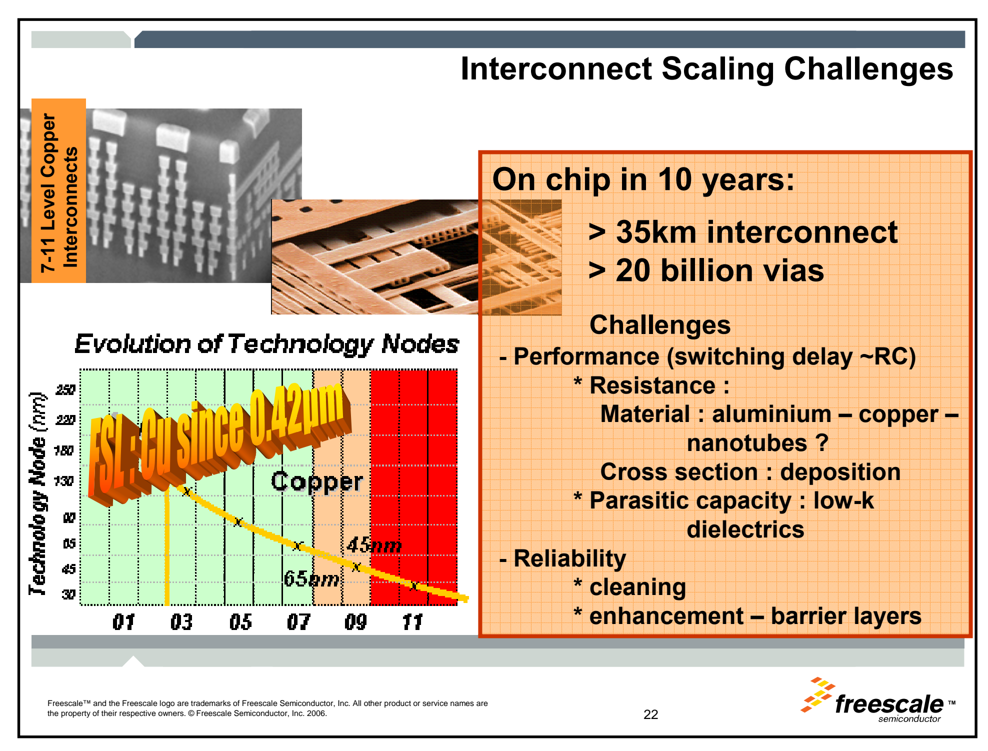
Interconnect Scaling Challenges
7-11 Level Copper Interconnects
On chip in 10 years:
> 35km interconnect
> 20 billion vias
Challenges
- Performance (switching delay ~RC)
* Resistance :
Material : aluminium – copper – nanotubes ?
Cross section : deposition
* Parasitic capacity : low-k dielectrics
- Reliability
* cleaning
* enhancement – barrier layers
Evolution of Technology Nodes
FSL : Cu since 0.42µm
Copper
45nm
65nm
Technology Node (nm)
250
220
180
130
90
65
45
30
01
03
05
07
09
11
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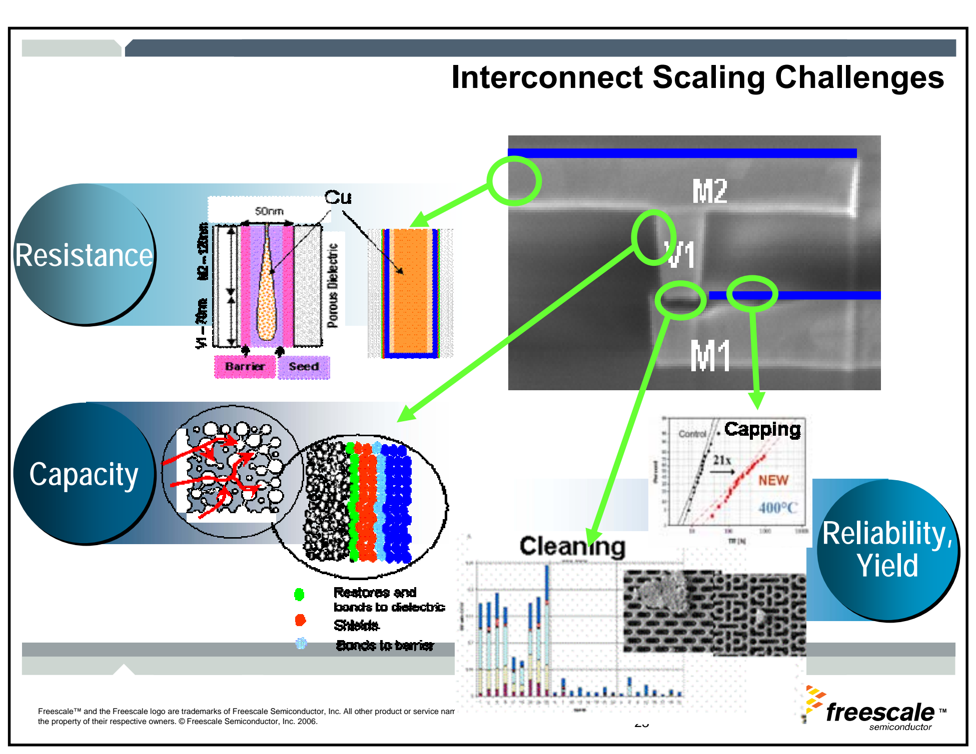
Interconnect Scaling Challenges
Resistance
Cu
50nm
M2 ~ 120nm
V1 ~ 70nm
Porous Dielectric
Barrier
Seed
M2
V1
M1
Capacity
Restores and bonds to dielectric
Shields
Bonds to barrier
Capping
Control
21x
NEW
400°C
Cleaning
Reliability, Yield
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"Sixty percent of fab-related (yield) problems are related to cleans, and another twelve percent to etching steps,"

Wide range of potential wafer cleaning technologies for robust volume production requirements at the 45nm node and below:

- incumbent : the ubiquitous RCA clean technique and its derivatives
- Shock tube-enhanced laser-induced plasma (LIP) shockwaves for sub-50 nm nanoparticle removal. This approach confines LIP beams to specially engineered "shock tubes" to increase the cleaning power of shock waves.
- Ionized molecular-activated coherent technology, which employs a charged solution of ammonia in water to form clusters that attract particles at the molecular level, without damaging the wafer surface.
- Particles removal by forming nanoscale bubbles to absorb the contaminants
- etc.…

2007 Surface Preparation and Cleaning Conference, organized by SEMATECH

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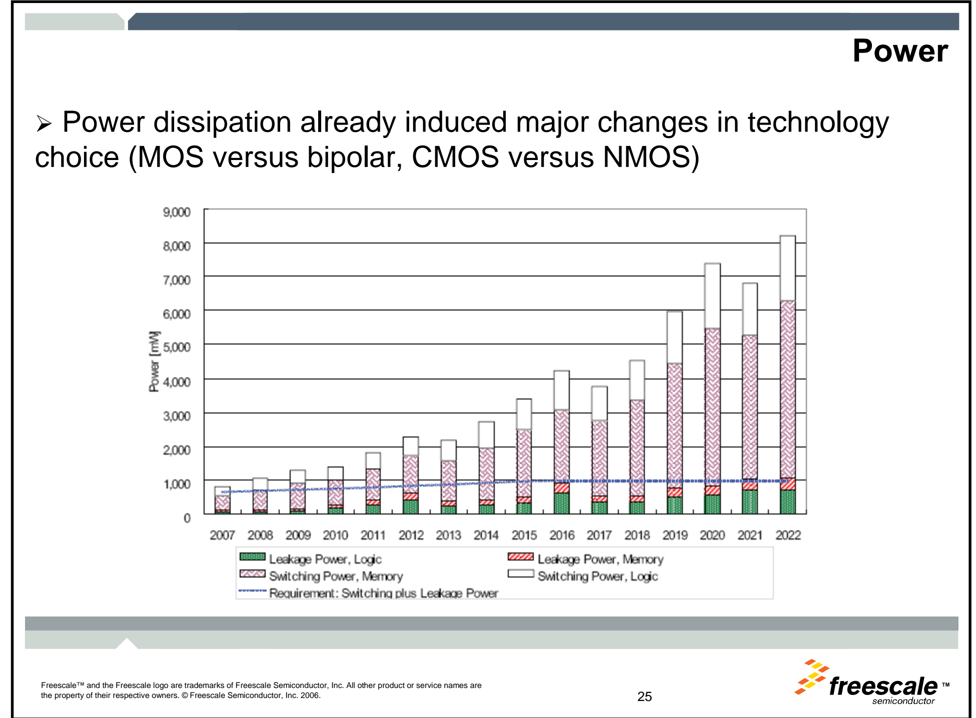
Power

➢ Power dissipation already induced major changes in technology choice (MOS versus bipolar, CMOS versus NMOS)



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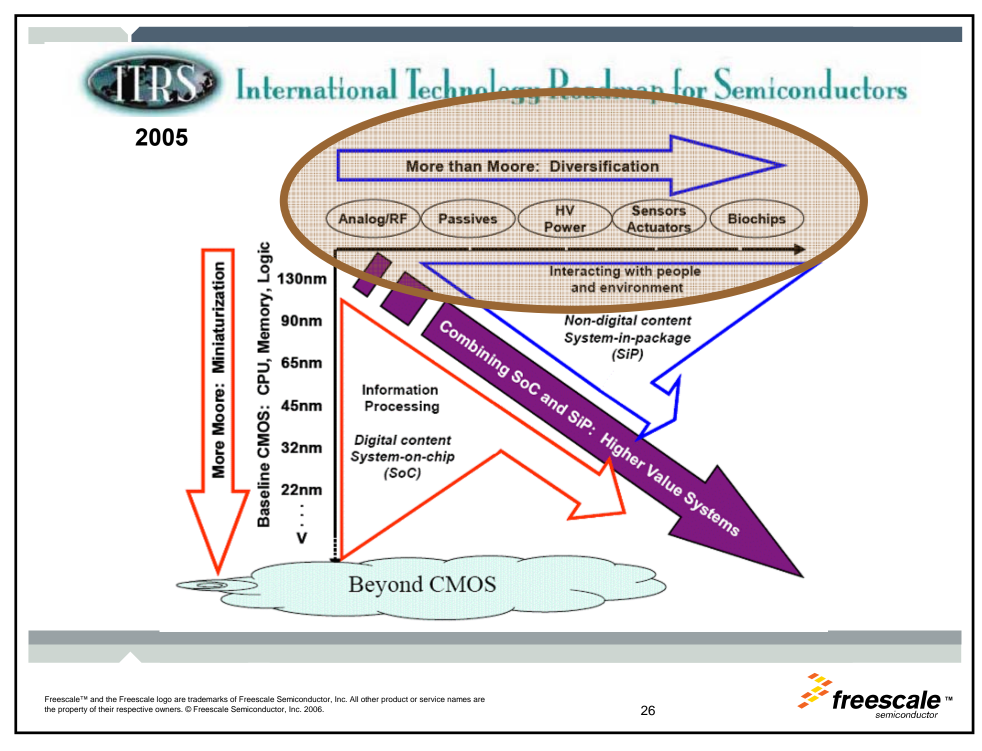
ITRS International Technology Roadmap for Semiconductors
2005
More than Moore: Diversification
Analog/RF
Passives
HV Power
Sensors Actuators
Biochips
Interacting with people and environment
Non-digital content System-in-package (SiP)
More Moore: Miniaturization
Baseline CMOS: CPU, Memory, Logic
130nm
90nm
65nm
45nm
32nm
22nm
V
Information Processing
Digital content System-on-chip (SoC)
Combining SoC and SiP: Higher Value Systems
Beyond CMOS
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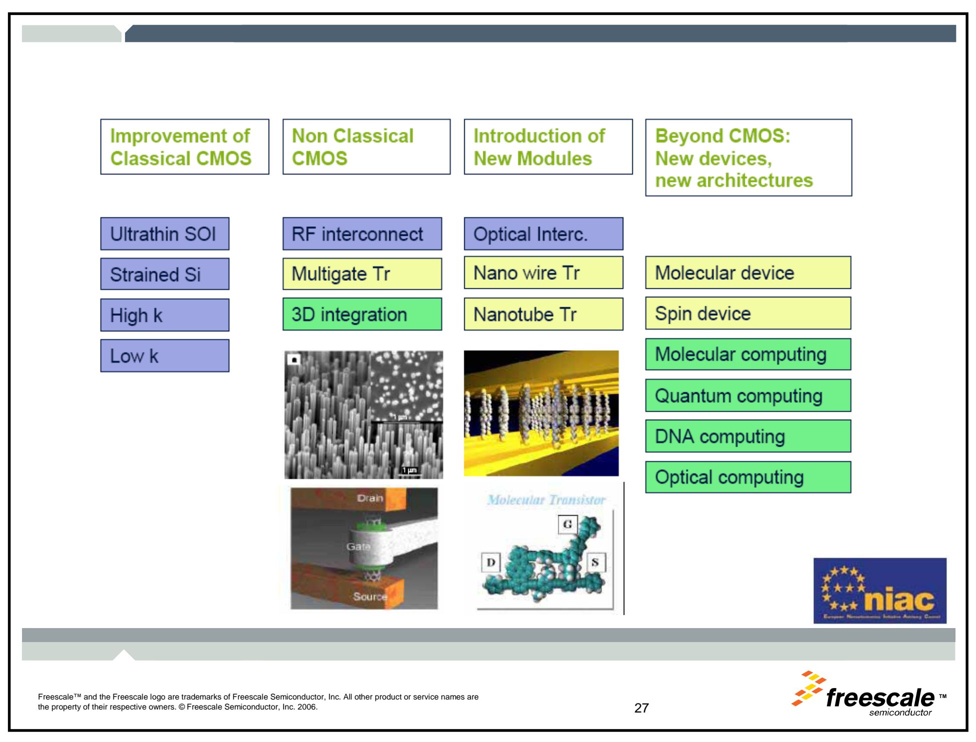
Improvement of Classical CMOS
Non Classical CMOS
Introduction of New Modules
Beyond CMOS: New devices, new architectures
Ultrathin SOI
Strained Si
High k
Low k
RF interconnect
Multigate Tr
3D integration
Optical Interc.
Nano wire Tr
Nanotube Tr
Molecular device
Spin device
Molecular computing
Quantum computing
DNA computing
Optical computing
Drain
Gate
Source
Molecular Transistor
G
D
S
niac
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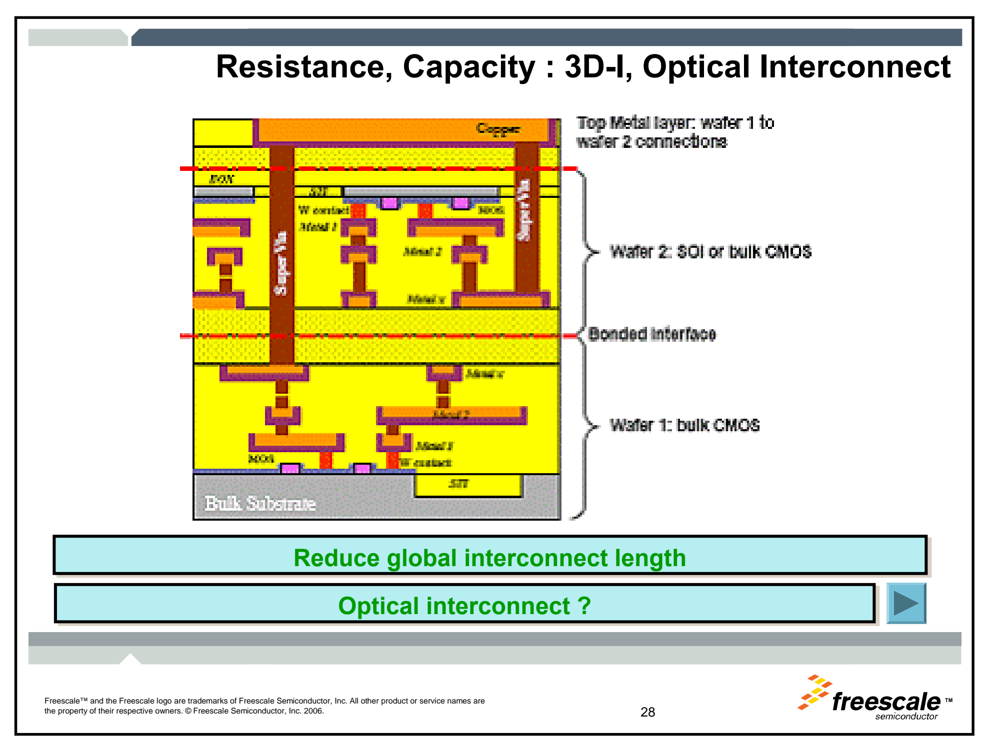
Resistance, Capacity : 3D-I, Optical Interconnect
Top Metal layer: wafer 1 to wafer 2 connections
Wafer 2: SOI or bulk CMOS
Bonded interface
Wafer 1: bulk CMOS
Bulk Substrate
Copper
SuperVia
Reduce global interconnect length
Optical interconnect ?
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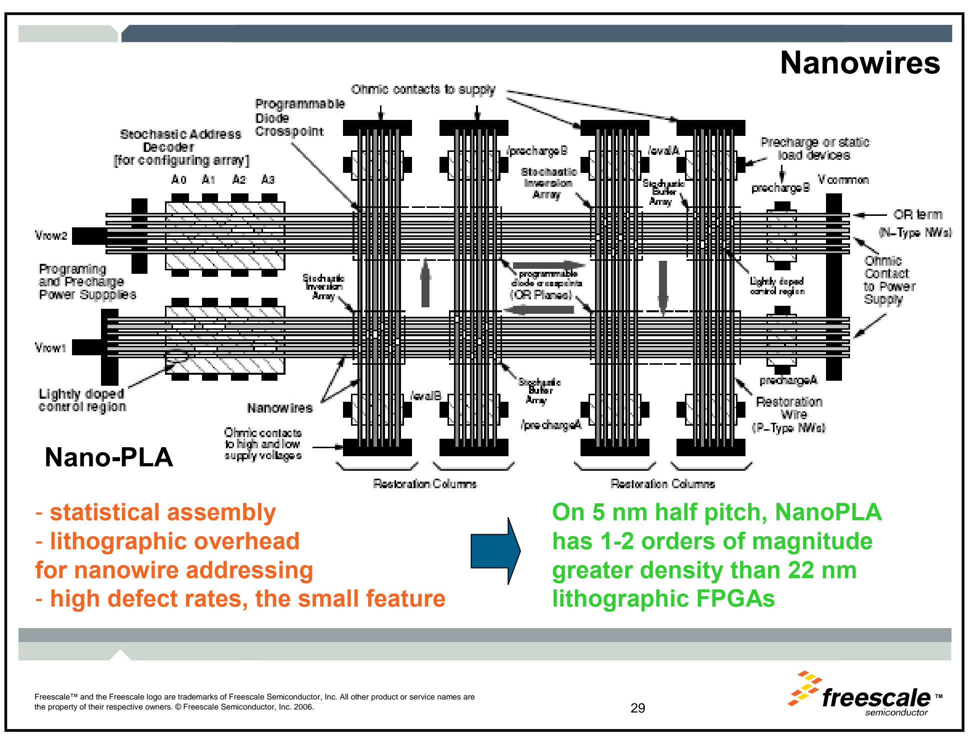
Nanowires
Ohmic contacts to supply
Programmable Diode Crosspoint
Stochastic Address Decoder [for configuring array]
A0 A1 A2 A3
Precharge or static load devices
Vrow2
Programing and Precharge Power Suppplies
Vrow1
Lightly doped control region
Nanowires
Ohmic contacts to high and low supply voltages
OR term (N-Type NWs)
Ohmic Contact to Power Supply
Restoration Wire (P-Type NWs)
Restoration Columns
Nano-PLA
- statistical assembly
- lithographic overhead
for nanowire addressing
- high defect rates, the small feature
On 5 nm half pitch, NanoPLA has 1-2 orders of magnitude greater density than 22 nm lithographic FPGAs
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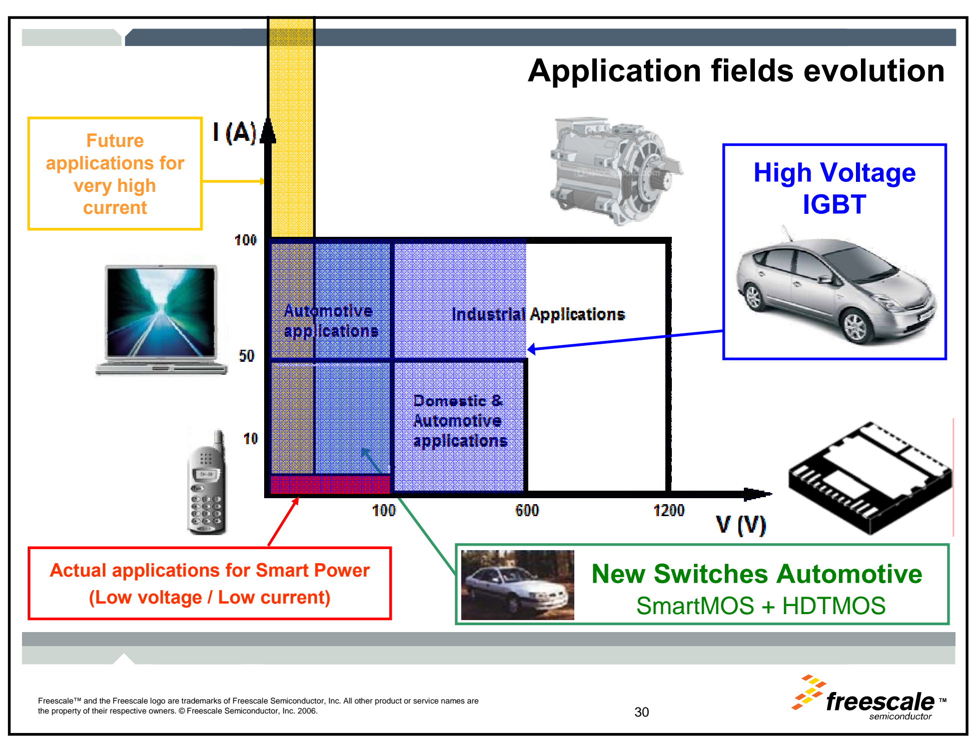
Application fields evolution
Future applications for very high current
I (A)
100
50
10
Automotive applications
Industrial Applications
Domestic & Automotive applications
100
600
1200
V (V)
High Voltage IGBT
Actual applications for Smart Power (Low voltage / Low current)
New Switches Automotive
SmartMOS + HDTMOS
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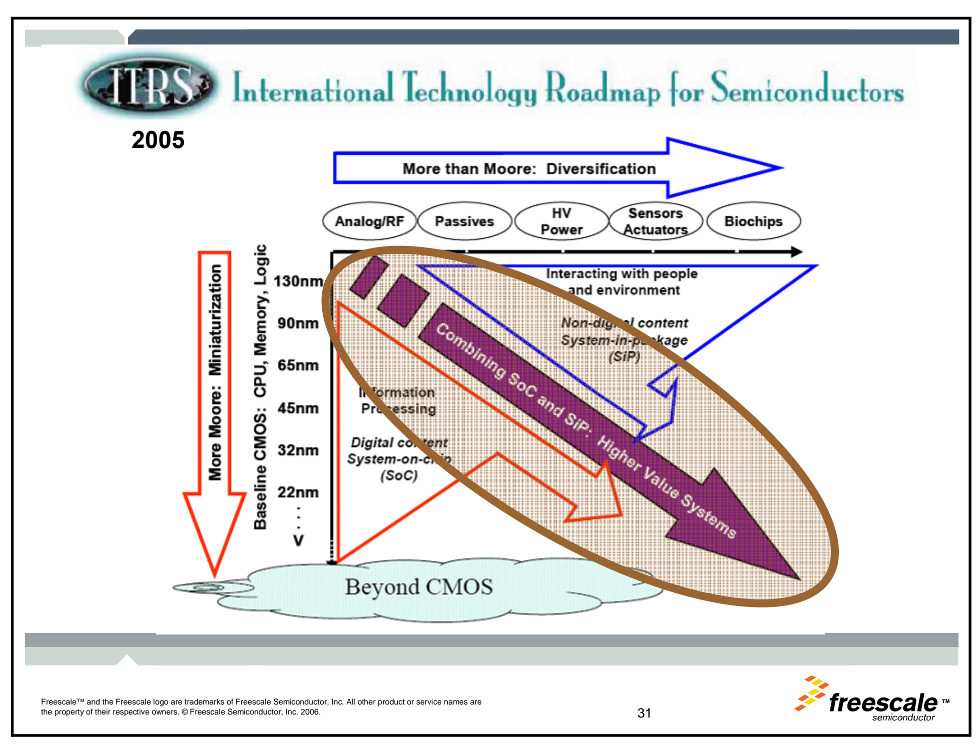
ITRS International Technology Roadmap for Semiconductors
2005
More than Moore: Diversification
Analog/RF
Passives
HV Power
Sensors Actuators
Biochips
More Moore: Miniaturization
Baseline CMOS: CPU, Memory, Logic
130nm
90nm
65nm
45nm
32nm
22nm
V
Interacting with people and environment
Non-digital content System-in-package (SiP)
Information Processing
Digital content System-on-chip (SoC)
Combining SoC and SiP: Higher Value Systems
Beyond CMOS
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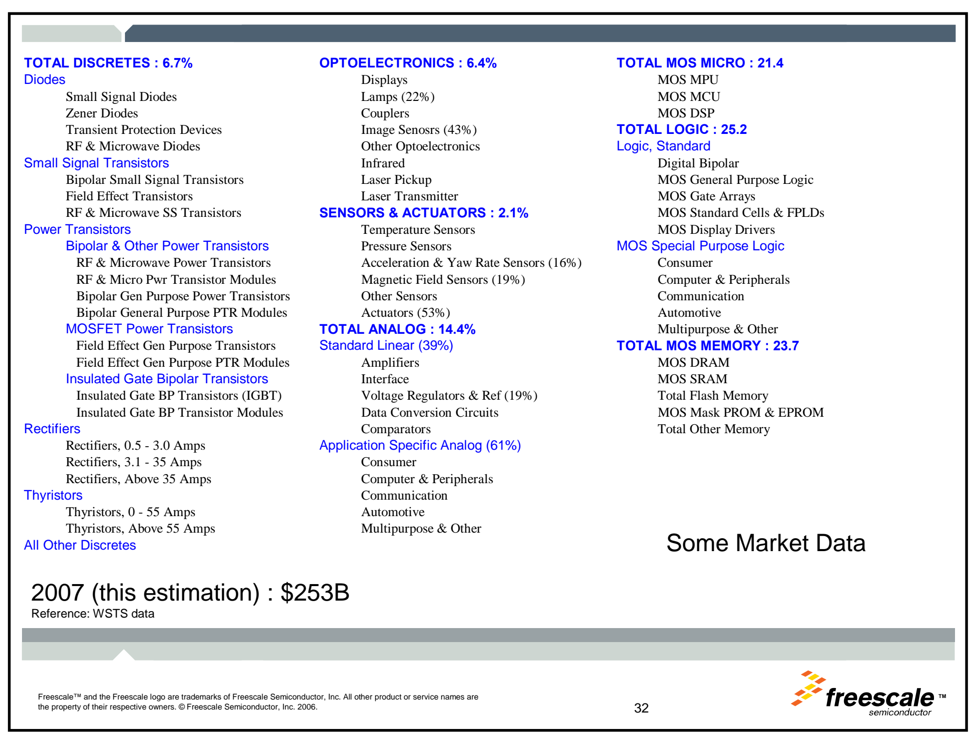
TOTAL DISCRETES : 6.7%
Diodes
Small Signal Diodes
Zener Diodes
Transient Protection Devices
RF & Microwave Diodes
Small Signal Transistors
Bipolar Small Signal Transistors
Field Effect Transistors
RF & Microwave SS Transistors
Power Transistors
Bipolar & Other Power Transistors
RF & Microwave Power Transistors
RF & Micro Pwr Transistor Modules
Bipolar Gen Purpose Power Transistors
Bipolar General Purpose PTR Modules
MOSFET Power Transistors
Field Effect Gen Purpose Transistors
Field Effect Gen Purpose PTR Modules
Insulated Gate Bipolar Transistors
Insulated Gate BP Transistors (IGBT)
Insulated Gate BP Transistor Modules
Rectifiers
Rectifiers, 0.5 - 3.0 Amps
Rectifiers, 3.1 - 35 Amps
Rectifiers, Above 35 Amps
Thyristors
Thyristors, 0 - 55 Amps
Thyristors, Above 55 Amps
All Other Discretes
OPTOELECTRONICS : 6.4%
Displays
Lamps (22%)
Couplers
Image Sensors (43%)
Other Optoelectronics
Infrared
Laser Pickup
Laser Transmitter
SENSORS & ACTUATORS : 2.1%
Temperature Sensors
Pressure Sensors
Acceleration & Yaw Rate Sensors (16%)
Magnetic Field Sensors (19%)
Other Sensors
Actuators (53%)
TOTAL ANALOG : 14.4%
Standard Linear (39%)
Amplifiers
Interface
Voltage Regulators & Ref (19%)
Data Conversion Circuits
Comparators
Application Specific Analog (61%)
Consumer
Computer & Peripherals
Communication
Automotive
Multipurpose & Other
TOTAL MOS MICRO : 21.4
MOS MPU
MOS MCU
MOS DSP
TOTAL LOGIC : 25.2
Logic, Standard
Digital Bipolar
MOS General Purpose Logic
MOS Gate Arrays
MOS Standard Cells & FPLDs
MOS Display Drivers
MOS Special Purpose Logic
Consumer
Computer & Peripherals
Communication
Automotive
Multipurpose & Other
TOTAL MOS MEMORY : 23.7
MOS DRAM
MOS SRAM
Total Flash Memory
MOS Mask PROM & EPROM
Total Other Memory
Some Market Data
2007 (this estimation) : $253B
Reference: WSTS data
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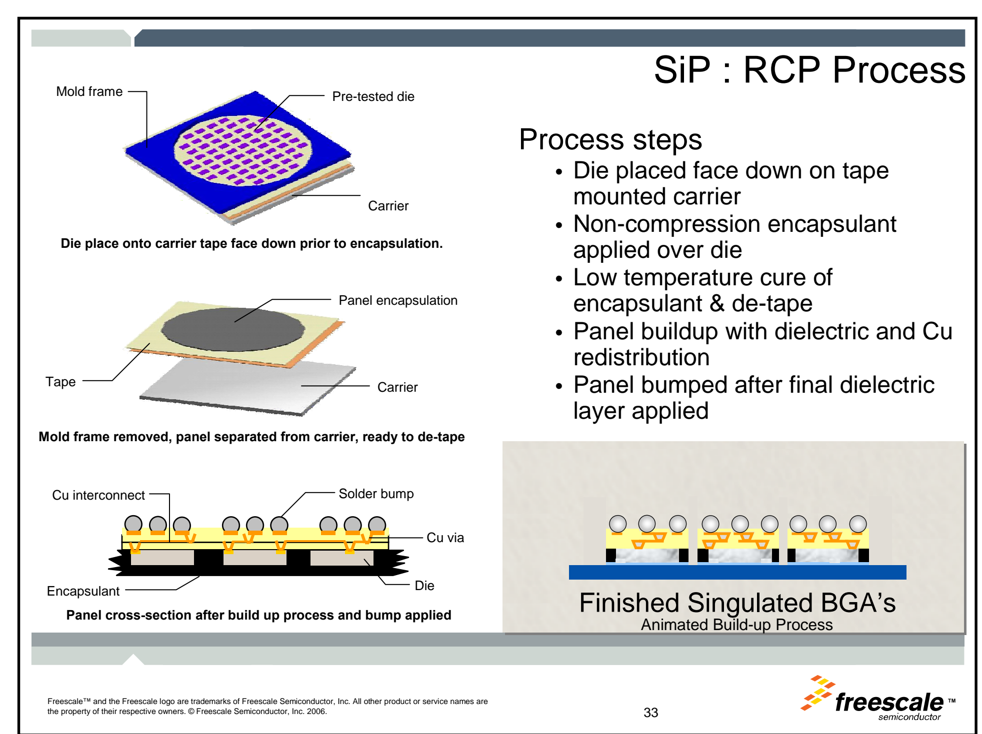
SiP : RCP Process
Mold frame
Pre-tested die
Carrier
Die place onto carrier tape face down prior to encapsulation.
Panel encapsulation
Tape
Carrier
Mold frame removed, panel separated from carrier, ready to de-tape
Cu interconnect
Solder bump
Cu via
Die
Encapsulant
Panel cross-section after build up process and bump applied
Process steps
• Die placed face down on tape mounted carrier
• Non-compression encapsulant applied over die
• Low temperature cure of encapsulant & de-tape
• Panel buildup with dielectric and Cu redistribution
• Panel bumped after final dielectric layer applied
Finished Singulated BGA's
Animated Build-up Process
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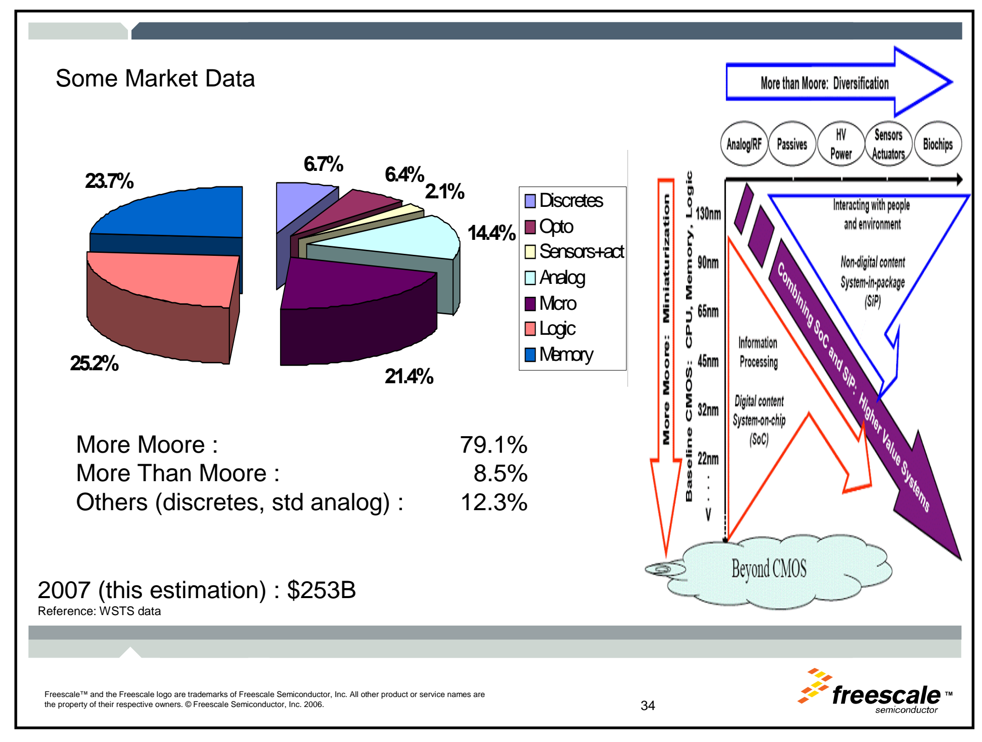
Some Market Data
23.7%
6.7%
6.4%
2.1%
14.4%
25.2%
21.4%
Discretes
Opto
Sensors+act
Analog
Micro
Logic
Memory
More Moore : 79.1%
More Than Moore : 8.5%
Others (discretes, std analog) : 12.3%
2007 (this estimation) : $253B
Reference: WSTS data
More than Moore: Diversification
Analog/RF
Passives
HV Power
Sensors Actuators
Biochips
More Moore: Miniaturization
Baseline CMOS: CPU, Memory, Logic
130nm
90nm
65nm
45nm
32nm
22nm
Interacting with people and environment
Non-digital content System-in-package (SiP)
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Digital content System-on-chip (SoC)
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Beyond CMOS
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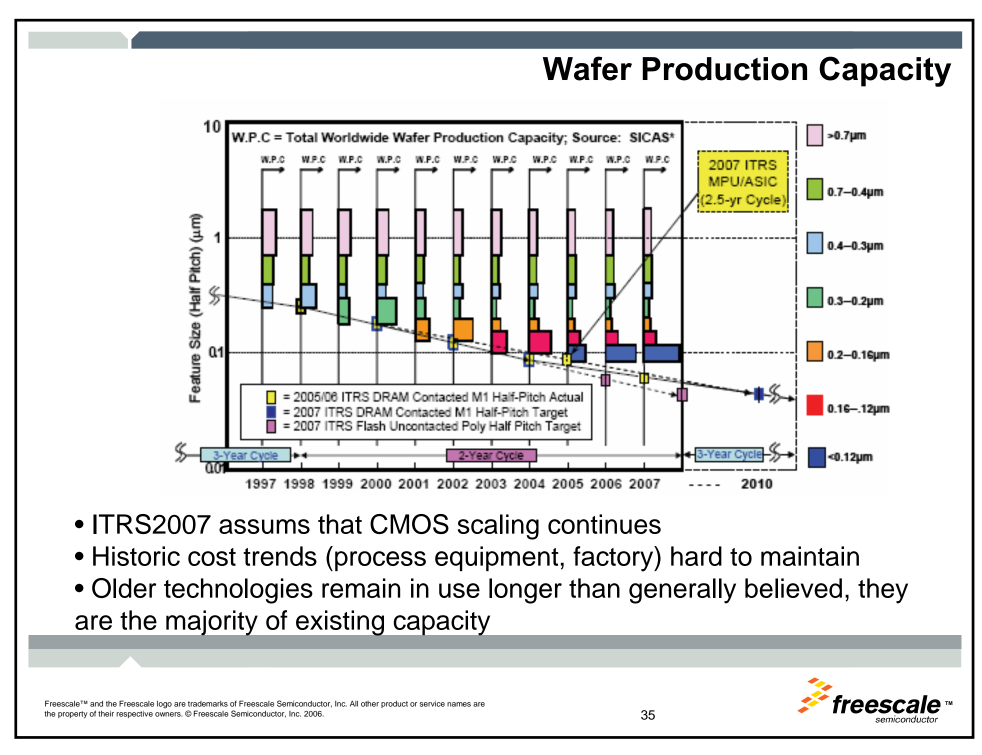
Wafer Production Capacity
W.P.C = Total Worldwide Wafer Production Capacity; Source: SICAS*
2007 ITRS MPU/ASIC (2.5-yr Cycle)
Feature Size (Half Pitch) (µm)
10
1
0.1
0.01
= 2005/06 ITRS DRAM Contacted M1 Half-Pitch Actual
= 2007 ITRS DRAM Contacted M1 Half-Pitch Target
= 2007 ITRS Flash Uncontacted Poly Half Pitch Target
3-Year Cycle
2-Year Cycle
3-Year Cycle
1997 1998 1999 2000 2001 2002 2003 2004 2005 2006 2007 ---- 2010
>0.7µm
0.7–0.4µm
0.4–0.3µm
0.3–0.2µm
0.2–0.16µm
0.16–.12µm
<0.12µm
• ITRS2007 assums that CMOS scaling continues
• Historic cost trends (process equipment, factory) hard to maintain
• Older technologies remain in use longer than generally believed, they are the majority of existing capacity
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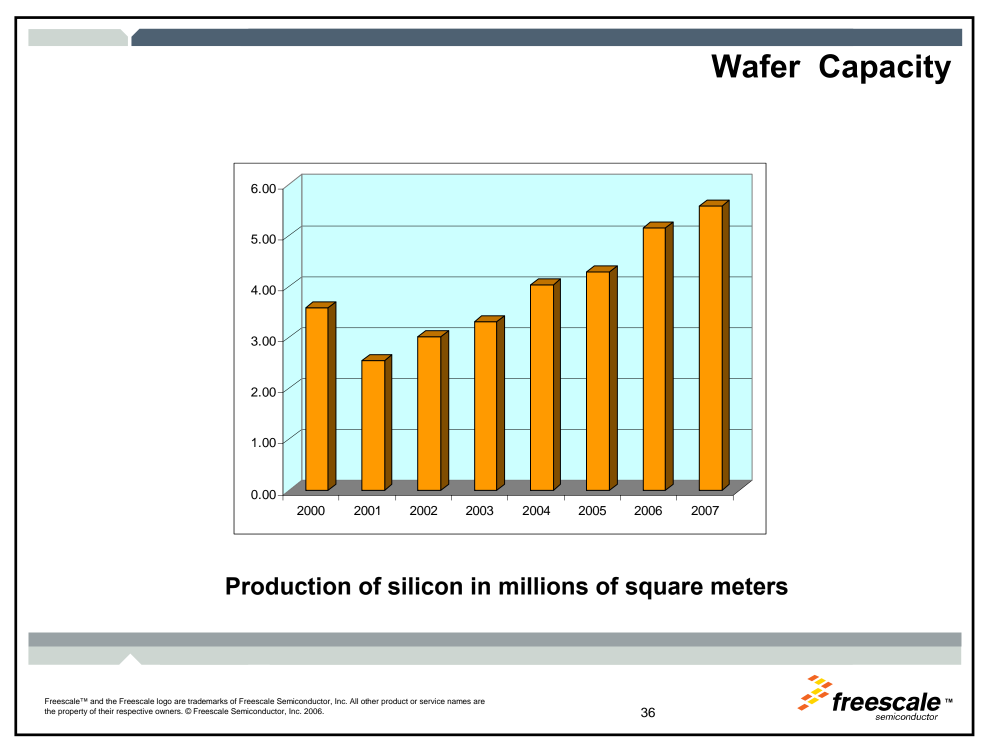

Wafer Capacity
6.00
5.00
4.00
3.00
2.00
1.00
0.00
2000
2001
2002
2003
2004
2005
2006
2007
Production of silicon in millions of square meters
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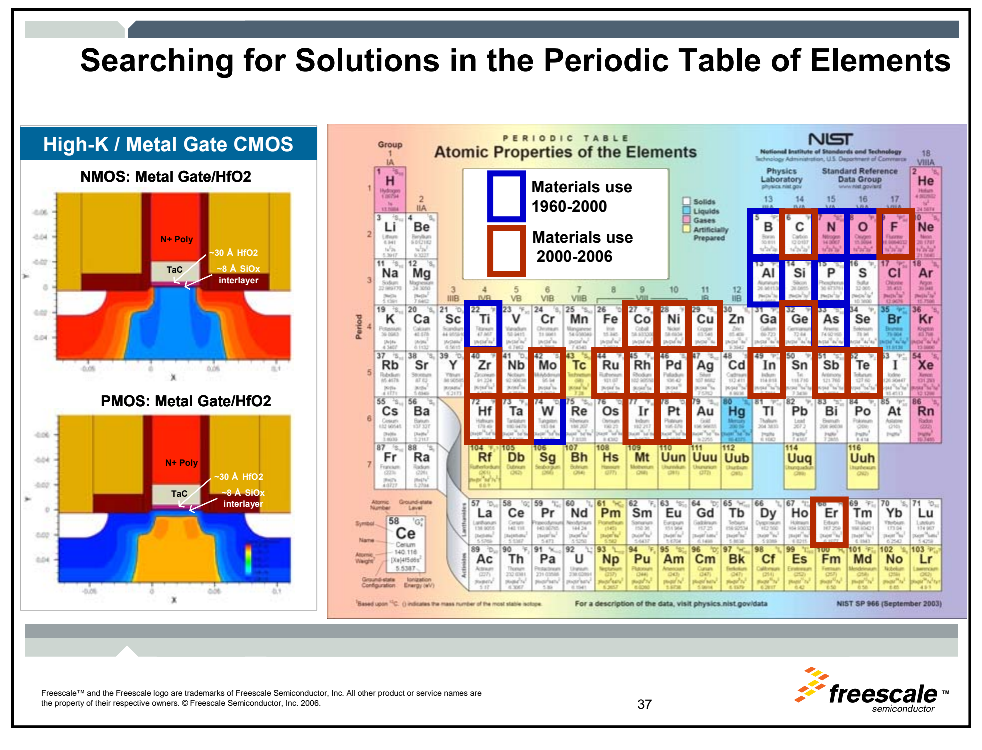

Searching for Solutions in the Periodic Table of Elements
High-K / Metal Gate CMOS
NMOS: Metal Gate/HfO2
N+ Poly
~30 Å HfO2
TaC
~8 Å SiOx interlayer
PMOS: Metal Gate/HfO2
Atomic Properties of the Elements
NIST
Materials use 1960-2000
Materials use 2000-2006
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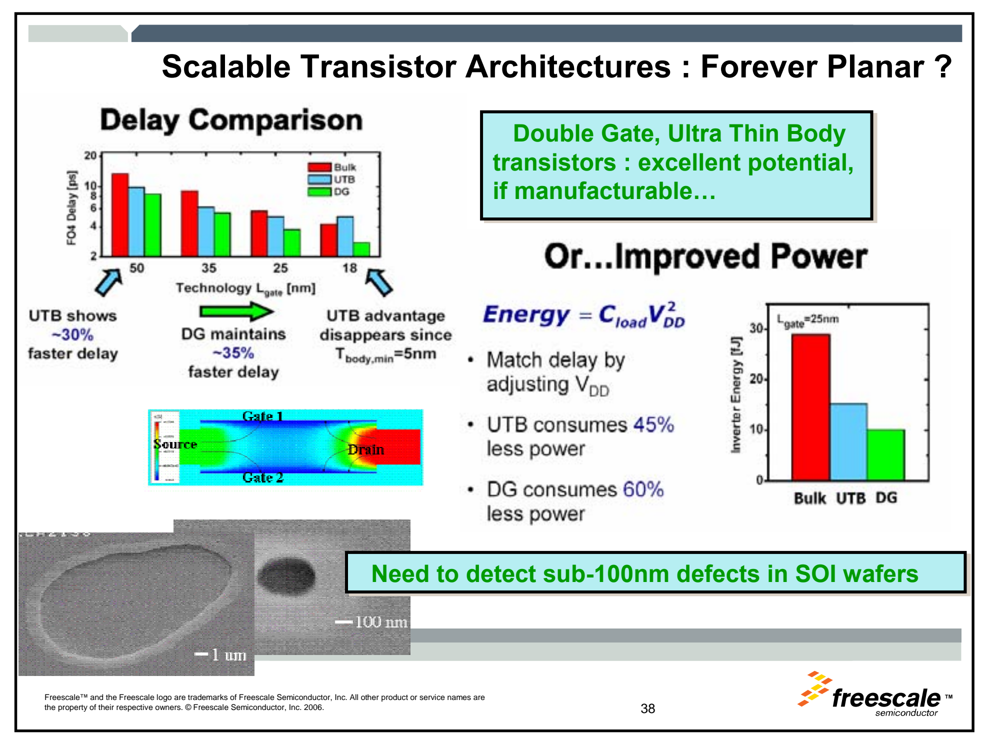
Scalable Transistor Architectures : Forever Planar ?
Delay Comparison
Bulk
UTB
DG
FO4 Delay [ps]
Technology L_gate [nm]
UTB shows ~30% faster delay
DG maintains ~35% faster delay
UTB advantage disappears since T_body,min=5nm
Double Gate, Ultra Thin Body transistors : excellent potential, if manufacturable…
Or…Improved Power
Energy = C_load V_DD^2
Match delay by adjusting V_DD
UTB consumes 45% less power
DG consumes 60% less power
L_gate=25nm
Inverter Energy [fJ]
Bulk UTB DG
Gate 1
Source
Drain
Gate 2
1 um
100 nm
Need to detect sub-100nm defects in SOI wafers
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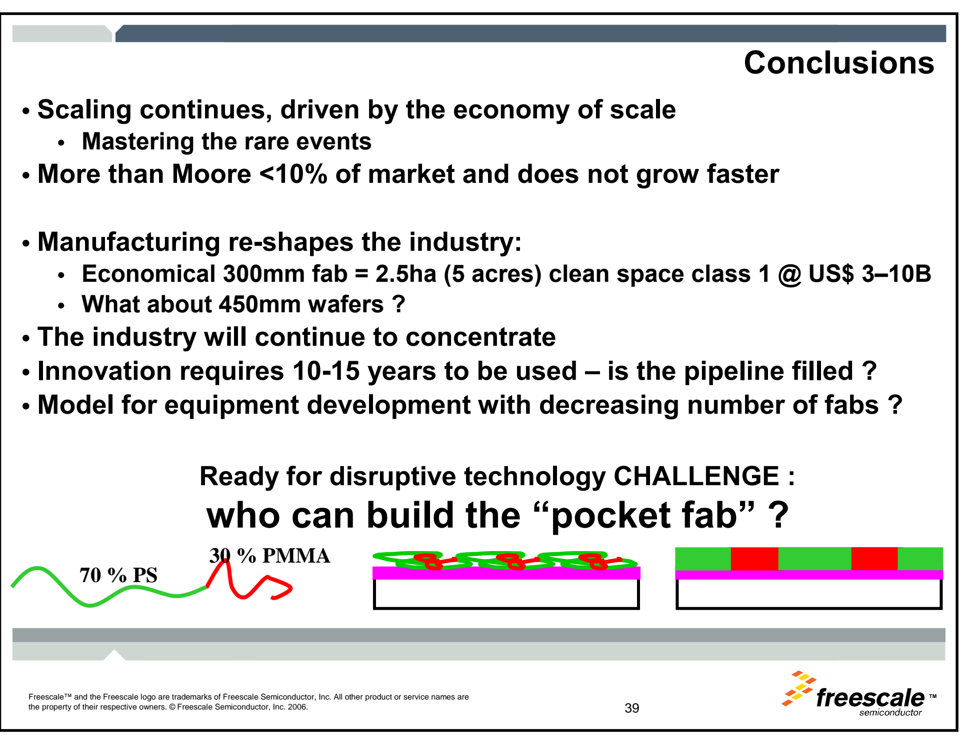
Conclusions
• Scaling continues, driven by the economy of scale
• Mastering the rare events
• More than Moore <10% of market and does not grow faster
• Manufacturing re-shapes the industry:
• Economical 300mm fab = 2.5ha (5 acres) clean space class 1 @ US$ 3–10B
• What about 450mm wafers ?
• The industry will continue to concentrate
• Innovation requires 10-15 years to be used – is the pipeline filled ?
• Model for equipment development with decreasing number of fabs ?
Ready for disruptive technology CHALLENGE :
who can build the “pocket fab” ?
70 % PS
30 % PMMA
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